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DATA BOOK 1995

STARTECH Component Data

Catalog

Printed September 8, 1994

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STARTECH Semiconductor Inc. 1215 BORDEAUX Dr. SUNNYVALE, CA 94089 TEL (408) 745-0801 FAX (408) 745-1269

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Startech's products are marketed and distributed through a world-class network of representatives and distributors.

At Startech, we are dedicated to keeping your designs competitive with leading edge solutions. All our products are low power, high performance, CMOS ICs. Our commitment to you is to provide you with high quality and reliable ICs.

Ram K. Reddy President



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Ram K. Reddy President

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FREQUENCY SYNTHESIZERS
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DIFFERENTIAL LINE DRIVERS Startech Semiconductor National Semiconductor DS26C31/DS26LS31 ST26C31 ST34C86 DS34C86/DS34LS86 AMD Startech Semiconductor ST26C31 AM26LS31 **DIFFERENTIAL LINE RECEIVERS** Startech Semiconductor National Semiconductor DS26C32/DS26LS32 ST26C32 DS34C87/DS34LS87 ST34C87 Startech Semiconductor AMD AM26LS32 ST26C32 DIFFERENTIAL LINE RECEIVERS / DRIVERS Motorola Semiconductor Startech Semiconductor MC34050 ST34C50 MC34051 ST34C51 UARTS National Semiconductor Startech Semiconductor INS8250A ST16C450 INS82C50A ST16C450 NS16450 ST16C450 NS16C450 ST16C450 NS16550AF ST16C550 NS16C552 ST16C2552 Silicon Systems Startech Semiconductor SSI73M550 ST16C550 SSI73M1550 ST16C1450 / ST16C1550 SSI73M2550 ST16C1451 / ST16C1551 SSI73M2551 ST16C1552 VLSI Technology, Inc. Startech Semiconductor VL82C50A ST16C450 VL16C450 ST16C450 VL16C550 ST16C550 Western Digital Inc. Startech Semiconductor WD16C450 ST16C450

ST16C550

WD16C550

CROSS REFERENCE LIST

Texas Instruments Startech Semiconductor TL16C450 ST16C450 TL16C550A ST16C550 **Exar Corporation** Startech Semiconductor XR16C450 ST16C450 XR16C550 ST16C550 **UARTS WITH PRINTER** VLSI Technology, Inc. Startech Semiconductor VL16C452 ST16C452 VL16C552 ST16C552 / ST16C553 Western Digital Inc. Startech Semiconductor WD16C452 ST16C452 ST16C552 / ST16C553 WD16C552 Texas Instruments Startech Semiconductor TL16C452 ST16C452 TL16C552 ST16C552 **Exar Corporation** Startech Semiconductor XR16C452 ST16C452 XR16C552 ST16C552 VIDEO DOT CLOCK GENERATOR Integrated Circuit Systems, Inc. Startech Semiconductor ICS2494XXX ST49C214-XX ICS9064 ST49C064 ICS9154-XX ST49C154-XX ICS9158 ST49C158 Avasem Corporation Startech Semiconductor AV9064 ST49C064 AV9103-XX ST49C103-XX AV9104-XX ST49C104-XX AV9106 ST49C106 AV9107-XX ST49C107-XX AV9155-XX ST49C155-XX STEREO CLOCK GENERATOR

Startech Semiconductor

ST49C418

MicroClock Inc.

MK1418

CROSS REFERENCE LIST

DIFFERENTIAL LINE DRIVERS

Startech Semiconductor ST26C31 National Semiconductor DS26C31/DS26LS31

AMD AM26LS31

ST34C86

National Semiconductor DS34C86/DS34LS86

DIFFERENTIAL LINE RECEIVERS

Startech Semiconductor ST26C32 National Semiconductor DS26C32/DS26LS32

AMD AM26LS32

ST34C87

National Semiconductor DS34C87/DS34LS87

DIFFERENTIAL LINE RECEIVERS / DRIVERS

Startech Semiconductor ST34C50 ST34C51 Motorola Semiconductor MC34050 MC34051

UARTS

Startech Semiconductor ST16C450

National Semiconductor INS8250A INS82C50A NS16450 NS16C450

VLSI Technology, Inc. VL82C50A VL16C450

Western Digital Inc. WD16C450

Texas Instruments TL16C450

Exar Corporation XR16C450

CROSS REFERENCE LIST

Startech Semiconductor ST16C550

National Semiconductor NS16550AF

Silicon Systems SSI73M550

VLSI Technology, Inc. VL16C550

Western Digital Inc. WD16C550

Texas Instruments TL16C550A

Exar Corporation XR16C550

Silicon Systems SSI73M1550

SSI73M2550

SSI73M2551

National Semiconductor NS16C552

VLSI Technology, Inc. VL16C452

Exar Corporation XR16C452

Western Digital Inc. WD16C452

Texas Instruments TL16C452

ST16C1450 ST16C1550

ST16C1451 ST16C1551

ST16C2552

ST16C2552

UARTS WITH PRINTER Startech Semiconductor ST16C452AT

ST16C452AT/PS

ST16C452AT/PS

CROSS REFERENCE LIST -

ST16C552/553

VLSI Technology, Inc. VL16C552

Exar Corporation XR16C552

Western Digital Inc. WD16C552

Texas Instruments TL16C552

VIDEO DOT CLOCK GENERATOR

Startech Semiconductor ST49C064

Avasem Corporation AV9064

Integrated Circuit Systems, Inc. ICS9064

Startech Semiconductor ST49C103-XX ST49C104-XX ST49C106

ST49C107-XX ST49C155-XX Avasem Corporation

AV9103-XX AV9104-XX AV9106 AV9107-XX AV9155-XX

ST49C154-XX ST49C158

Startech Semiconductor ST49C214-XX

Integrated Circuit Systems, Inc.

ICS9154-XX ICS9158

Integrated Circuit Systems, Inc. ICS2494XXX

STEREO CLOCK GENERATOR Starech Semiconductor

ST49C418

MicroClock Inc. MK1418

CROSS REFERENCE LIST:

ST19C552/S53

VLSI Tachnology, Inc. VL180552

Exar Corporation XR16C552

Western Digital Inc. WiD16C552

Texas instruments TL160552

Avasam Corporation AV9084

Integrated Circuit Systems, Inc. ICS9064

Avesem Corporation
AV9103-XX
AV9106
AV9106
AV9107-XX

Integrated Circuit Systems, Inc. ICS2494XXX

MicroClock Inc. Mic1418 VIDEO DOT CLOCK GENERATOR Startech Semiconductor STASCOSA

> Startech Semiconductor ST49C103-XX BT49C104-XX ST49C106 BT49C107-XX BT49C155-XX

> > ST49C154-XX

Startech Semiconductor

STERED CLOCK GENERATOR Sterech Semiconductor ST49C418 FREQUENCY SYNTHESIZERS 1

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ST49C001

Printed September 2, 1994

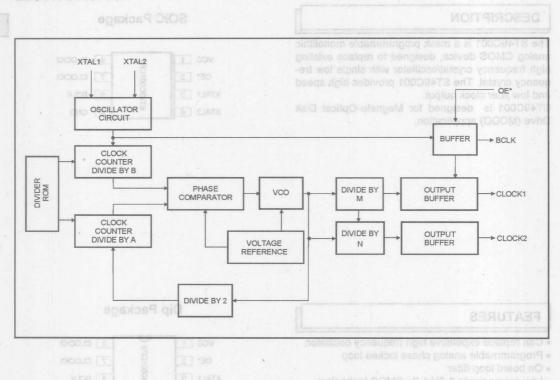
PREPROGRAMMED HIGH SPEED FREQUENCY SYNTHESIZER

DESCRIPTION **SOIC Package** The ST49C001 is a mask programmable monolithic analog CMOS device, designed to replace existing VCC 1 8 CLOCK2 ST49C001CF8 high frequency crystal/oscillator with single low fre-OE* 2 7 CLOCK1 quency crystal. The ST49C001 provides high speed and low jitter clock output. XTAL1 3 6 BCLK ST49C001 is designed for Magneto-Optical Disk XTAL2 4 5 GND Drive (MODD) appplication. Dip Package **FEATURES** · Can replace expensive high frequency oscillator. 8 CLOCK2 ST49C001CP8 Programmable analog phase locked loop OE* 2 7 CLOCK1 On board loop filter XTAL1 3 6 BCLK • Low power single 3-5V 1.2μ CMOS technology • 8 pin SOIC package. XTAL2 4 5 GND · Crystal oscillator circuit on board

ORDERING INFORMATION

Part number ST49C001CF8 Package SOIC Operating temperature 0° C to +70° C PREPROGRAMMED HIGH SPEED FREQUENCY SYNTHESIZER

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description		
VCC	1	I	Analog supply voltage. Single +3 /+5 volts.		
OE*	2*		Output Enable (Active low). CLOCK1 and BCLK outputs are disabled and forced to low state when this pin is low. CLOCK2 output pin is active when CLOCK1 and BCLK outputs are disabled.		
XTAL1	3 annu	Limite Typ Max	Crystal or External Clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 16.9344 MHz clock XTAL2 is left open or used as buffered clock output.		
XTAL2	4 V	· 8.0 o	Crystal output.		
GND Am 0.8 = 10	5	0 0.4	Digital ground.		
BCLK VINO C NIC	6	001-0	Buffered reference clock output.		
CLOCK1	7 Am	20 0 30	Preprogrammed 50 MHz clock output.		
CLOCK2	8	0	Preprogrammed 30 MHz clock output.		

^{*} Has internal pull-up resistor

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup, it is recommended to connect 0.047µF capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C001 contains an analog phase locked loop circuit with digital closed loop dividers and a final output divider to achieve the desired dividing ratios for the clock output.

The accuracy of the frequencies produced by the ST49C001 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLOCK1	=	(Reference	clock)	X	2A/B X	1/M
CLOCK2	=	(Reference	clock)	X	2A/B X	1/N

where	A=5, 6, 7,128
	B=5, 6, 7,128
	M=1, 2,6
	N=1, 2,6

Output Frequencies				
49.143 MHz				
29.486 MHz				

ABSOLUTE MAXIMUM RATINGS

7 Volts
GND-0.3 V to VCC+0.3 V
0° C to +70° C
-40° C to +150° C
500 mW
Signal Type

DC ELECTRICAL CHARACTERISTICS

 T_A =0-70° C, Vcc=3.0 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
V _{IL} V _{IH} V _{OL} V _{OH} I _{IL} I _{IH} I _{CC}	5.0 Volts operation Input low level Input high level Output low level Output high level Input low current Input high current Operating current	2.0	20	0.8 0.4 -100 1 30	V V V V PA PA MA	I _{OL} = 8.0 mA I _{OH} = 8.0 mA Pin 2 only V _{IN} =Vcc Pin 2 No load. CLOCK=50MHz
V _I L V _O L V _O L V _O H IIL IIL CC	3.0 Volts operation Input low level Input high level Output low level Output high level Input low current Input high current Operating current Input pull-up resistance	2.0	15	0.6 0.4 -100 1 20	V V V μA μA mA	I _{OL} = 2.0 mA I _{OH} = 2.0 mA Pin 2 only V _{IN} =Vcc Pin 2 No load. CLOCK=50MHz

AC ELECTRICAL CHARACTERISTICS

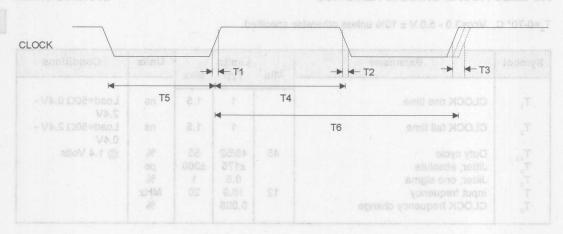
 T_a =0-70° C, Vcc=3.0 - 5.0 V ± 10% unless otherwise specified.

Parameter	Limits Min Typ Max				Conditions
CLOCK rise time	T4	1	1.5	≅⊺ ns	Load=50Ω 0.4V - 2.4V
CLOCK fall time		. 1	1.5	ns	Load=50Ω 2.4V - 0.4V
Duty cycle Jitter, absolute	45	48/52 ±175	55 ±300	% ps	@ 1.4 Volts
Jitter, one sigma Input frequency	12	0.5 16.9	1 20	MHz	
	CLOCK rise time CLOCK fall time Duty cycle Jitter, absolute Jitter, one sigma Input frequency	CLOCK rise time CLOCK fall time Duty cycle Jitter, absolute Jitter, one sigma	Min Typ CLOCK rise time 1 CLOCK fall time 1 Duty cycle 45 48/52 Jitter, absolute ±175 Jitter, one sigma 0.5 Input frequency 12 16.9	Min Typ Max CLOCK rise time 1 1.5 CLOCK fall time 1 1.5 Duty cycle 45 48/52 55 Jitter, absolute ±175 ±300 Jitter, one sigma 0.5 1 Input frequency 12 16.9 20	Min Typ Max CLOCK rise time 1 1.5 ns CLOCK fall time 1 1.5 ns Duty cycle 45 48/52 55 % Jitter, absolute ±175 ±300 ps Jitter, one sigma 0.5 1 % Input frequency 12 16.9 20 MHz

ST49C001

ST49C001

TIMING DIAGRAM





ST49C064

Printed September 2, 1994

PREPROGRAMMED DUAL VIDEO/MEMORY FREQUENCY GENERATOR

GENERAL DESCRIPTION

The ST49C064 is a monolithic analog CMOS device designed to generate dual frequency outputs from fifteen possible combinations for video Dot clock frequencies and eight memory clock frequencies for high performance video display systems. The ST49C064 is a mask option programmable device to provide different output frequencies for custom applications. It is designed with 1.2µ process to achieve 130 MHz speed for high end frequencies.

The ST49C064 is designed to replace existing video clocks generated from individual oscillators, to reduce board space and number of oscillators. To provide high speed and low jitter clock, The ST49C064 utilizes high speed analog CMOS phase locked loop using 14.318 MHz system clock as reference clock (reference clock can be changed to generate optional frequencies from standard programmed device).

The ST49C064 can provide optional clock frequencies, utilizing single layer metal mask option. The programmed clock outputs are selectable via four address lines and address latch enable pin for video Dot clock selection and three address lines for memory clock selection.

FEATURES

- Can replace multiple oscillators/crystals
- Pin -to-pin compatible to ICS90C64
- Programmable analog phase locked loop
- High speed (up to 130 MHz output)
- Low power single 5V CMOS technology
- 20 pin dip / SOIC / PLCC packages
- Compatible with Western Digital Imaging Video Graphics Array clock requirements.

ORDERING INFORMATION

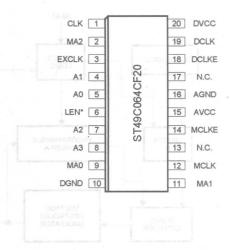
 Part number
 Package
 Operating temperature

 ST49C064CP20-xx
 Plastic-DIP
 0° C to +70° C

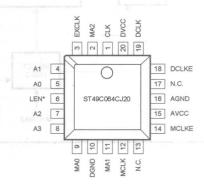
 ST49C064CF20-xx
 SOIC
 0° C to +70° C

 ST49C064CJ20-xx
 PLCC
 0° C to +70° C

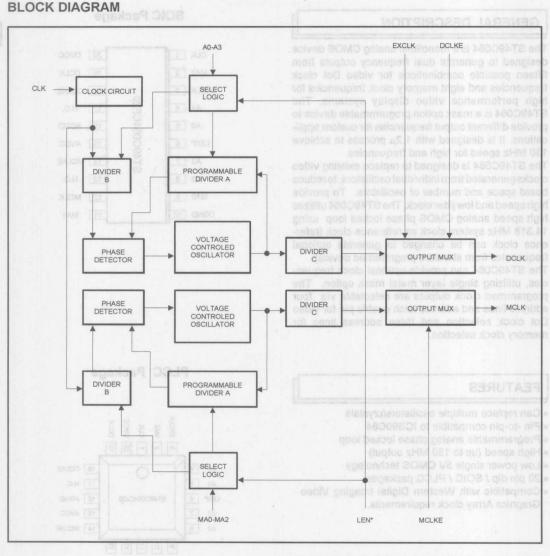
SOIC Package



PLCC Package



1



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CLK	1	Enallschi I	External 14.318 MHz system reference clock input.
MA2	be in any deco	ny frequency car DLIK, cah control	Memory clock Frequency select address 3.
EXCLK	3*	1	External clock input. For additional clock frequency.
A1	4*	1	Dot clock Frequency select address 2.
A0	5*	1	Dot clock Frequency select address 1.
LEN*	6*	1	Address latch enable input (active low). To latch selected programmed clock output.
A2	7*	1	Dot clock Frequency select address 3.
A3	8*	1	Dot clock Frequency select address 4.
MA0	9*	1	Memory clock Frequency select address 1.
DGND	10	0	Digital ground.
MA1	11*	1	Memory clock Frequency select address 2.
MCLK	12	0	Programmed memory clock output frequency.
N.C.	13		No connect. (© (%A) X (deplo accessions as a
MCLKE	14*	1 =	MCLK output enable.
AVCC	15	. 1	Analog supply voltage. Single +5 volts.
AGND	16	0	Analog ground.
N.C.	17		No connect. a addicate of type and addicate of the state
DCLKE	18*	1	DCLK output enable.
DCLK	19	0	Programmed video clock output frequency.
DVCC	20	1	Digital supply voltage. Single +5 volts.

^{*} Have internal pull-up resistors on inputs

GENERAL INFORMATION

The ST49C064 is programmed to generate 15 different video clock frequencies using the A0-A3 inputs and 8 different memory frequencies using M0-M2 inputs. The address lines A2-A3 can be connected to video controller like Western Digital Imaging VGA controllers. Address lines A0 and A1 are latched with LEN* pin which is generated from video controllers to select proper Dot clock output. All inputs to the ST49C064 contain internal pull-up resistors including CLK and EXCLK inputs.

The EXCLK is additional input that may be internally connected to the DCLK output. The additional input is useful for supporting modes that require frequencies not provided by the ST49C064.

FREQUENCY SELECT CALCULATION

The ST49C064 contains an analog phase locked loop circuit with a digital closed loop divider and a final series divider to achieve desired dividing ratios for clock output.

The accuracy of the frequencies produced by the ST49C064 depends on the input frequency and final output frequency. The formula for calculating the exact output frequency is as follows:

DCLK = (Reference clock) X (A/B.C) MCLK = (Reference clock) X (A/B.C)

where A=1,2,3,......127, B=1,2,3,......127, and B agallov vique polariA C=1,2,4

For proper output frequency, the ST49C064 can accept reference frequency from 5 - 40 MHz and divider ratio up to 15.

MASK OPTIONS

The following mask options are provided for custom applications.

- * Any frequency can be in any decoding position.
- * DCLK, can control selection of the internal frequencies.

ABSOLUTE MAXIMUM RATINGS

Supply range 7 Volts
Voltage at any pin GND-0.3 V to VCC+0.3 V
Operating temperature 0° C to +70° C
Storage temperature -40° C to +150° C
Package dissipation 500 mW

DC ELECTRICAL CHARACTERISTICS

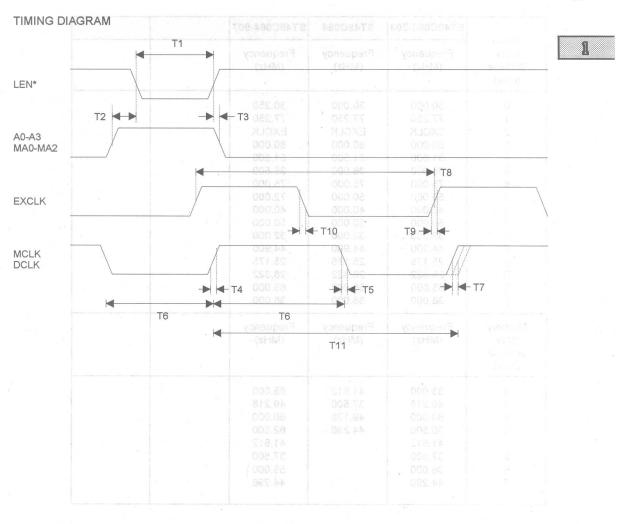
 $T_{\Delta}=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
V _{IL} V _{IH} V _{OL}	Input low level Input high level Output low level	2.0		0.8	V	I _{OL} = 8.0 mA
V _{OH} I _{IL} I _{IH} I _{CC}	Output high level Input low current Input high current Operating current	2.4	20	-350 1 30	V μΑ μΑ mA	I _{OH} = 8.0 mA V _{IN} =Vcc No load. DCLK=80MHz,
R _{in}	Internal pull-up resistance	15	20	25	kΩ	MCLK=40MHz

AC ELECTRICAL CHARACTERISTICS

 T_A =0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	2 12 2	Parameter				Min	Limits Typ	Max	Units	Conditions	
Ţ,	Enable pu			20 20 10	stics	ASTO	ns ns	IC ELECTRICAL			
12	T ₂ Setup time data to e Hold time to data en Rise time Fall time Duty cycle Duty cycle Jitter										
T ₄ T ₅ T ₆			enable				1 1 48/52	1.5 1.5 60	ns ns ns %	0.8V - 2.0V 2.0V - 0.8V 1.4V switch point	
T ₆	Duty cycle Jitter	etint)				45	48/52 ±175	55 ±300	% ps	Vcc/2 swite	
T ₈ T ₉ T ₁₀ T ₁₁ Am	Input frequence input clock input clock Output fre	k rise tim k fall tim	е		0	14.318	0.005	32 20 20	MHz ns ns %	input low Input high	
Am	lon = 8.0	V Au	-350		4	2	h			Output his	Vor
										Input high Operating	



1-15

\	ST49C064-903	ST49C064	ST49C064-907		
Video clock address (Hex)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)		
. 0	30.000	30.000	30.250		The same
1	77.250	77.250	77.250		T2 (4-b)
2	EXCLK	EXCLK	EXCLK	1	
3	80.000	80.000	80.000	7	
4	31.500	31.500	31.500		
5	36.000	36.000	35.500	- 10	
6	75.000	75.000	75.000		
7	50.000	50.000	72.000	1	
8	40.000	40.000	40.000	No. 1	
9	50.000	50.000	50.000		
Α	32.000	32.000	32.000		
В	44.900	44.900	44.900		
С	25.175	25.175	25.175		
D	28.322	28.322	28.322		1
E		65.000		M M-	
F	36.000	36.000	36.000	p-14	- P -
Memory	Frequency	Frequency	Frequency	(D)	
clock	(MHz)	(MHz)	(MHz)		
address					
(Hex)					
0	33.000	41.612	65.000		
1	49.218	37.500	49.218	A STATE OF	
2	60.000	49.128	60.000		The state of
3	30.500	44.296	62.500		
4	41.612		41.612		
5	37.500		37.500		
6	36.000		55.000		
7	44.296		44.296		

Compatible with ICS9064-903 Video Controller WD90C30 AV9064 WD90C30 ICS9064-907 WD90C33



ST49C101CP8

ST49C101CF8

ST49C102CT8

SOIC

TSSOP

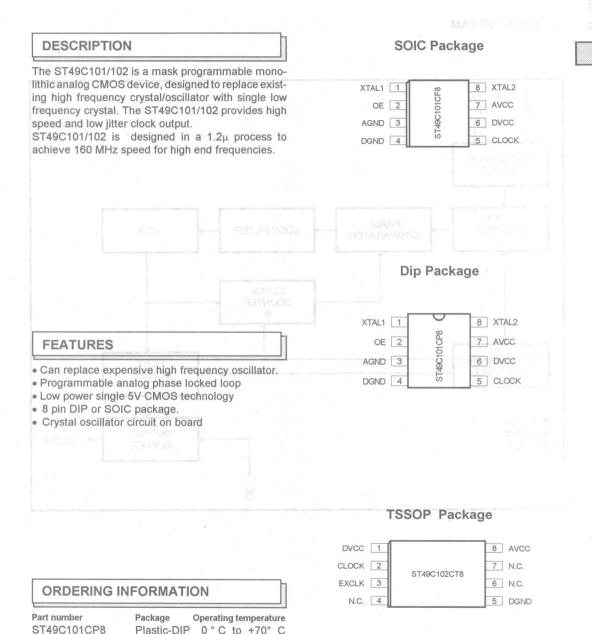
0° C to +70° C

0° C to +70° C

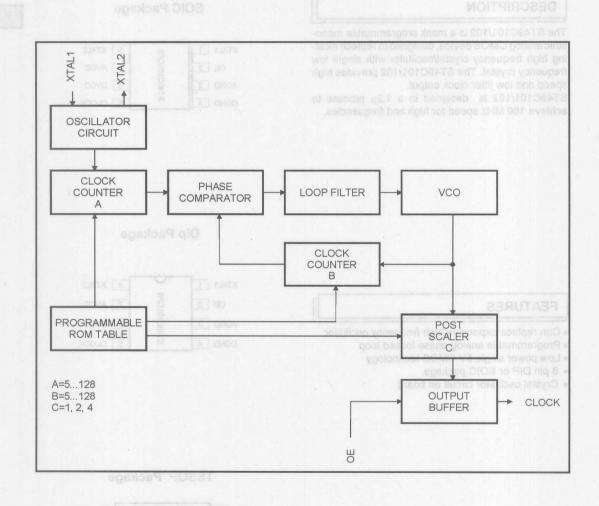
ST49C101/102

Printed September 2, 1994

PREPROGRAMMED HIGH SPEED FREQUENCY MULTIPLIER



BLOCK DIAGRAM



SYMBOL DESCRIPTION (ST49C101)

Symbol	Pin	Signal Type	Pin Description						
XTAL1	1	1	Crystal or External Clock input. A crystal can be connect to this pin and XTAL2 pin to generate internal phase lock loop reference clock. For external 10.00 MHz clock, XTA is left open or used as buffered clock output.						
OE	2*	T.	Clock Output Enable (Active high). CLOCK output is three stated when this pin is low.						
AGND	3	0	Analog ground. I grillalisoles as support est some trans-						
DGND	4	0	Digital ground.						
CLOCK	5	0	Programmed output clock.						
DVCC	6	1	Positive supply voltage. Single +5 volts.						
AVCC	7	1	Analog supply voltage. Single +5 volts.						
XTAL2	8	0	Crystal output. 4 0% 5 mont yoursupan a seek as a seek						

^{*} Has internal pull-up resistor

SYMBOL DESCRIPTION (ST49C102)

Symbol	Pin	Signal Type	Pin Description							
DVCC	1 .	1	Digital Positive supply voltage. Single +5 volts.							
CLOCK	2	0	Pre-programmed output clock.							
EXCLK	3	1	External Clock input. Input reference clock.							
DGND	5	0	Digital ground.							
AVCC	8	1 1	Analog supply voltage. Single +5 volts.							

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup, it is recommended to connect 0.047µF capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C101/102 contains an analog phase locked loop circuit with digital closed loop dividers and a final output divider to achieve the desired dividing ratios for the clock output. So is an ideal and a second a second and a second and a second and a second and a second an

The accuracy of the frequencies produced by the ST49C101/102 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLOCK = (Reference clock) X 2A/(BXC)

where A=5, 6, 7,.....128

B=5, 6, 7,......128 C=1,2,4

For proper output frequency, the ST49C101/102 can accept a reference frequency from 7 - 20 MHz and divider ratio up to 15.

Preprogrammed options:

ST49C101-X	Factor	Max. Output Frequency
ST49C101-01	12	100 MHz
ST49C101-02	6	100 MHz
ST49C101-03	8	160 MHz
ST49C101-04	4	100 MHz

ST49C102	Input Frequency	Output Frequency
ST49C102	40MHz	60MHz

500 mW

ABSOLUTE MAXIMUM RATINGS 10 101020ATE) 20172193 10A0AFD JACTEST 1

Supply range Voltage at any pin GND-0.3 V to VCC+0.3 V 0° C to +70° C Operating temperature -40° C to +150° C Storage temperature Package dissipation

DC ELECTRICAL CHARACTERISTICS

 $T_A=0-70^{\circ}$ C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
V _{IL} V _{IH}	Input low level			0.8	V	
V _{IH}	Input high level Output low level	2.0		0.5	V	I _{oL} = 8.0 mA
V _{OL} V _{OH}	Output high level Input low current	2.8	STICS	-100	V μA	I _{OH} = 8.0 mA Pin 2 only
I	Input high current			1	μΑ	V _{IN} =Vcc Pin 2
l _{cc}	Operating current	speame	60	80	mA	No load. CLOCK=100MHz
R _{IN}	Input pull-up resistance	50	75	100	KΩ	

AC ELECTRICAL CHARACTERISTICS

 T_{Δ} =0 - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
	0.01		1	ESPECIAL SE	vonauna vonauna	I NOOJO
T ₁	CLOCK rise time	1,	1.5	2	ns	Load=50Ω 0.5V - 2.8V
T ₂	CLOCK fall time		1.5	2	ns	Load=50Ω 2.8V - 0.5V
T,	Duty cycle	40	48/52	60	%	1.4V switch point
, T ₅	Duty cycle	45	48/52	55	%	VCC/2 switch poin
T ₅ T ₃ T _{IN}	Jitter		±175	±300	ps	
T	Input reference frequency	7	10	20	MHz	
Tout	Output frequency			160	MHz	
T ₆	CLOCK frequency change		0.01	- /	%	

ST49C101/102

DC ELECTRICAL CHARACTERISTICS (ST49C101-02 and -04 ONLY)

 $T_a=0-70^{\circ}$ C, Vcc=3.0V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
V _{IL} V _{IH}	Input low level Input high level	2.0	eare	0.8	V	C EL ECTRICAL
VIL VIH VOL VOH	Output low level Output high level Input low current	2.0	simerwis	0.5	V V µA	I _{OL} = 4.0 mA I _{OH} = 4.0 mA Pin 2 only
I _{IH}	Input high current Operating current		40	60	μA mA	V _{IN} =Vcc Pin 2 No load. CLOCK=80 MHz
R _{IN}	Input pull-up resistance	50	75	100	ΚΩ	CLOCK OUT WITE

AC ELECTRICAL CHARACTERISTICS (ST49C101-02 and -04 ONLY)

 $T_a=0-70^{\circ}$ C, Vcc=3.0V ± 10% unless otherwise specified.

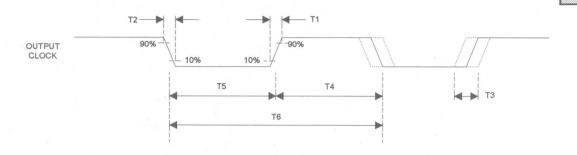
Symbol	Parameter	Min	Limits Min Typ		Units	Conditions	
T ₁	CLOCK rise time		1.5	2	ns	Load=50Ω 0.5V - 2.0V	
T ₂	CLOCK fall time	specifie	1.5	2 aaalnu.	ns 2001 z V	Load=50Ω 2.0V - 0.5V	
T ₅	Duty cycle	45	48/52	55	%	VCC/2 switch point	
T ₃ T _{IN} T _{OUT}	Jitter Input reference frequency	7	±175	±300 20	ps MHz	Symbol	
T _{OUT} T ₆	Output frequency CLOCK frequency change		0.01	80	MHz %	T. CLOOK-r	

ST49C101/102

ST49C101/102

TIMING DIAGRAM

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TIMING DIAGRAM



ST49C103 ST49C104

Printed September 2, 1994

PREPROGRAMMED FREQUENCY GENERATOR

DESCRIPTION

The ST49C103 and ST49C104 are mask programmable monolithic analog CMOS devices designed to generate up to 8 single frequency outputs from a single input clock. The ST49C104 will provide eight different output frequencies and the ST49C103 will provide four different output frequencies. They are designed in a 1.2µ process to achieve 130 MHz speed for high end frequencies.

The ST49C103 and ST49C104 are designed to replace existing video clocks generated from individual oscillators in order to reduce board space and number of oscillators. To provide high speed and low jitter clock, the parts utilize a high speed analog CMOS phase locked loop using 14.318 MHz system clock as the reference clock (note that reference clock can be changed to generate optional frequencies from a standard programmed device). The programmed clock outputs are selectable via three address lines and address latch enable pin. The ST49C104 also includes a power on reset circuit which will cause the select logic to select the frequency at address "000" upon power up. The latch enable pin is also mask programmable to be active high, active low or rising or falling edge sensitive.

FEATURES

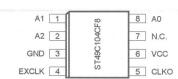
- Can replace up to 8 oscillators/crystals and a multiplexer
- Pin-to-pin compatible to Avasem AV9103/104
- Programmable analog phase locked loop
- Low power single 5V CMOS technology
- 8 or 14 pin DIP or SOIC package.

ORDERING INFORMATION

						0000000
Part number	Package	Opera	atin	g te	mperati	ure
ST49C103CP8	Plastic-DIP	0°	C	to	+70°	С
ST49C103CF8	SOIC	0°	C	to	+70°	C
ST49C104CP8	Plastic-DIP	0°	C	to	+70°	C
ST49C104CF8	SOIC	0°	C	to	+70°	C
ST49C104CP14	Plastic-DIP	0 °	C	to	+70°	C
ST49C104CF14	SOIC	0°	C	to	+70°	C

SOIC Package

	A1 1		14 A0
	A2 2	4	13 N.C.
	LEN 3	ICF14	12 AVCC
	GND 4	104	11 DVCC
NOTA:	OGND 5	ST49C	10 CLKO
. ×	TAL1 6	ST	9 CLK2
×	TAL2 7		8 CLK1

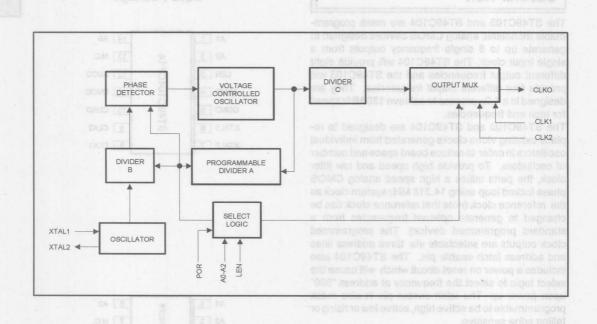




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STARTECH

BLOCK DIAGRAM



SYMBOL DESCRIPTION (ST49C104 14 pin package)

Symbol	Pin	Signal Type	Pin Description
A1	1 18	select address in	Frequency select address input 2.
A2	2*	select audress lap	Frequency select address input 3.
LEN	3*	l be	Address latch enable input. To latch selected programmed clock output.
AGND	tis koot easting 4	ek input. Internal O	Analog ground.
DGND	5	d outpro clock	Digital ground.
XTAL1	6 1 6		to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	7	ni azerbas loslas	Crystal output.
CLK1	8	1	External clock 1 input.
CLK2	9		External clock 2 input / output select.
CLKO	10	0	Programmed output clock.
DVCC	11	1 -	Digital supply voltage. Single +5 volts.
AVCC	12	T	Analog supply voltage. Single +5 volts.
N.C.	13		
A0	14	1	Frequency select address input 1.

^{*} Have internal pull-up resistors on inputs.

ST49C103/104

SYMBOL DESCRIPTION (ST49C104 8 pin package) MORES MORE MORE MANAGEMENT MORE MORE MORE MORE MANAGEMENT MORE MORE MORE MANAGEMENT MORE MANAGEMENT MORE

Symbol	Pin	Signal Type	Pin Description	toomyth
A1	1 15 fig	elect address in	Frequency select address input 2.	
A2	2* 8 his	ielēct alldress irg	Frequency select address input 3.	
GND menong	o laidi 8 electe	h enatO input.	Digital ground.	EN
EXCLK	4	l .bn	External clock input. Internal phase locked lo clock .	op reference
CLKO	5	0 br	Programmed output clock.	
phase looked		demail disck input d XTAL2 pin to p nce clock. For		
A0	s buffered clos	n beau to nego f	Frequency select address input 1.	

^{*}Has internal pull-up resistor on input

*Has internal pull-up resistor on input

*External clock 1 input

*External clock 2 input / output select.

*OLKC 10 O Programmed output clock

*OVC 11 Output supply voltage. Single +5 volts.

*Analog supply voltage. Single +5 volts.

SYMBOL DESCRIPTION (ST49C103 8pin package)

Symbol	Pin Signal Type		Pin Description
A1 .wol evidos	e active high or be in any decod	ton Enable can I	Frequency select address input 2.
	ni bebulanı edir. die ile obligete		Digital ground.
XTAL1	3	nal fraquencies	Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	4	0	Crystal output.
CLKO	5	0	Programmed output clock.
VCC	6	T	Digital supply voltage. Single +5 volts.
N.C.	7 7		- 48, 22, 18 - 8aP
Α0	8	1	Frequency select address input 1.

ST49C103/104

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect $0.047\mu F$ capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C104 contains an analog phase locked loop circuit with digital closed loop dividers and a final output multiplexer to achieve the desired dividing ratios for the clock output.

The accuracy of the frequencies produced by the ST49C104 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLKO = (Reference clock) X A/(B.C)

where

A=1,2,3,......127 B=8, 16, 32,64 C=1,2,4,8

MASK OPTIONS

The following mask options are provided for custom applications.

- * Latch Enable can be edge triggered or level sensitive.
- * Latch Enable can be active high or active low.
- * Any frequency can be in any decoding position.
- * CLK 1 and CLK 2 can be included in decoding table.
- * CLK2 can control selection of either CLK 1 or the internal frequencies.

For proper output frequency, the ST49C104 can accept a reference frequency from 5 - 40 MHz and divider ratio up to 15.

FEATURE	ST49C104 14-pin	ST49C104 8-pin	ST49C103 8-pin	
8 output frequencies	X	X		
4 output frequencies			X	
Programmable LEN pin	X	X	X	
Clock input only		X		
Crystal or clock input	X		X	
CLK1, CLK2 available for output mux	X			

Address latch (LEN)	State						
ST49C104-1 ST49C104-2 ST49C104-3	Transparent for LEN high Transparent for LEN low Transparent for LEN low						
	an			20.			

Supply range Voltage at any pin Operating temperature Storage temperature Package dissipation 7 Volts GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

DC ELECTRICAL CHARACTERISTICS

 T_{Δ} =0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
V _{IL}	Input low level			0.8	V	
V _{IH}	Input high level Output low level	2.0		0.4	V	1 - 8 0 m/
V _{OL} V _{OH}	Output high level	2.4		0.4	V	$I_{OL} = 8.0 \text{ mA}$ $I_{OH} = 8.0 \text{ mA}$
I	Input low current			-350	μА	Except crystal input
I _{IH}	Input high current			1	μА	V _{IN} =Vcc
Icc	Operating current		20	30	mA	No load.
R _{IN}	Input pull-up resistance	15	20	25	KΩ	DCLK=80MHz

ST49C103/104

AC ELECTRICAL CHARACTERISTICS

 T_{Δ} =0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

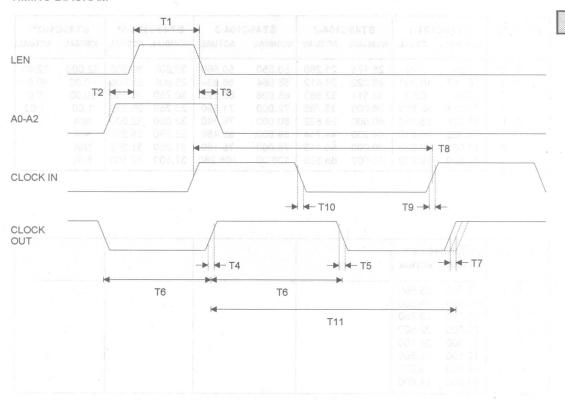
Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
						CANIDERID
T,	Enable pulse width	20			ns	
T,	Setup time data to enable	20			ns	
T ₃	Hold time to data enable	10			ns	
T,	Rise time		1	1.5	ns	0.8V - 2.0V
T,	Fall time		1	1.5	ns	2.0V - 0.8V
T _e	Duty cycle	40	48/52	60	%	1.4V switch point
T ₆	Duty cycle	45	48/52	55	%	Vcc/2 switch point
T,	Jitter		±175	±300	ps	
T ₈	Input frequency	14.318		32	MHz	
T _o	Input clock rise time			20	ns	
T_{2} T_{3} T_{4} T_{5} T_{6} T_{6} T_{7} T_{8} T_{10}	Input clock fall time			20	ns	SOLITE MAXIE
T ₁₁	Output frequency change		0.005		%	and the second

		put high current perating current	

ST49C103/104

ST49C103/104

TIMING DIAGRAM



A2 A1 A0		A0	ST490	104-1	ST49C104-2		ST490	104-3	ST49C	104-5*	ST49C103**		
			NOMINAL	ACTUAL	NOMINAL	ACTUAL	NOMINAL	ACTUAL	NOMINAL	ACTUAL	NORMAL	ACTUA	
0	0	0	Xtal	Xtal	25.175	25.280	50.350	50.560	39.000	39.000	32.000	32.00	
0	0	1	16.257	16.331	28.322	28.412	56.664	56.824	25.000	25.000	40.00	40.00	
0	1	0	Clk2	Clk2	32.514	32.663	65.028	65.326	30.750	30.750	50.00	50.00	
0	1	1	32.514	32.663	36.000	35.795	72.000	71.590	26.250	26.250	1.00	1.00	
1	0	0	25.175	25.056	40.000	39.822	80.000	79.640	32.000	32.000	N/A		
1	0	1	28.322	28.412	44.900	44.744	89.800	89.488	25.250	25.250	N/A		
1	1	0	24.000	23.938	50.000	50.113	75.000	75.169	31.250	31.250	N/A		
1	1	1	40.000	39.822	65.000	65.326	108.00	108.280	37.500	37.500	N/A		

A2 A1 A0	ST49C104-6** NOMINAL ACTUAL		27 - 4 - 4		
0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0	25.500 25.500 16.500 16.500 20.750 20.750 22.500 22.500 24.500 24.500 19.500 19.500 15.000 15.000 14.000 14.000	EET .	er	at .	

Input clock frequency = 14.318 MHz
* Input clock frequency = 16.0 MHz
** Input clock frequency = 8.0 MHz



ST49C106

Printed September 2, 1994

PREPROGRAMMED FREQUENCY GENERATOR

DESCRIPTION

The ST49C106 is a mask programmable monolithic analog CMOS device designed to generate up to 8 single frequency outputs from a single input clock. The ST49C106 is designed in a 1.2μ process to achieve 130 MHz speed for high end frequencies.

The ST49C106 is designed to replace existing video clocks generated from individual oscillators in order to reduce board space and number of oscillators. To provide high speed and low jitter clock, the parts utilize a high speed analog CMOS phase locked loop using 14.318 MHz system clock as the reference clock (note that reference clock can be changed to generate optional frequencies from a standard programmed device). The programmed clock outputs are selectable via three address lines and address latch enable pin. The ST49C106 also includes a power on reset circuit which will cause the select logic to select the frequency at address "000" upon power up. The ST49C106 contains de-glitch circuit so that full clock cycles are provided whenever the HALT pin stops or starts the output clock.

SOIC Package

A1 1	1	14 A0
A2 2	4	13 N.C.
LEN 3	ST49C106CF14	12 AVCC
AGND 4	901:	11 DVCC
DGND 5	490	10 CLKO
XTAL1 6	ST	9 HALT
XTAL2 7		8 SEL

Plastic-DIP package

FEATURES

- Can replace up to 8 oscillators/crystals and a multiplexer
- Pin-to-pin compatible to Avasem AV9106-14
- Programmable analog phase locked loop
- Low power single 5V CMOS technology
- 14 pin DIP or SOIC package.

ORDERING INFORMATION

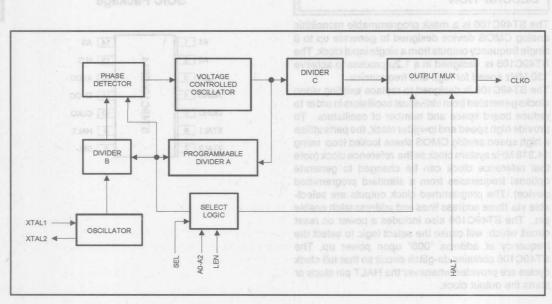
Part number Package Operating temperature
ST49C106CP14 Plastic-DIP 0 ° C to +70° C
ST49C106CF14 SOIC 0 ° C to +70° C

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REPROGRAMMED PREQUENCY GENERATOR

BLOCK DIAGRAM



Plastic-DIP package



FEATURES

- Can replace up to 8 oscillators/crystals and a multiplexer
 - Pin-to-pin compatible to Avasem AV9106-1
 - Programmable analog phase locked loop
 - Low power single 5V CMOS technology
 - of a pin OIP or SOIC package.

ORDERING INFORMATION

ast number Package Operating temperature
T#9C 106CP14 Plastic-DIP 0 ° C 10 +70° C

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
A1	1 12.3 12.3	C = (Reference L A	Frequency select address input 2.
A2	2*	8 I	Frequency select address input 3.
LEN	3*	L and tenters recomm	Address latch enable input. To latch selected programmed clock output.
AGND	- a morty/oneur	a refeorce fre	Analog ground.
DGND	5	0	Digital ground.
XTAL1	6	Ī	Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	7 7	-0	Crystal output.
SEL SE	8	1	Clock level select / CLK1. When HALT is asserted, SEL selects whether the clock is high or low. This level must be selected before the clock is halted. SEL pin can be used as an xternal clock input when HALT is active.
HALT	9	1	Start / Stop output clock.
CLKO	10	0	Programmed output clock.
DVCC	11 email	Jupiter Light	Digital supply voltage. Single +5 volts.
AVCC	12	8.0 1	Analog supply voltage. Single +5 volts.
Α0	14	A 0 I	Frequency select address input 1.

^{*} Have internal pull-up resistors on inputs.

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect 0.047 μ F capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C106 contains an analog phase locked loop circuit with digital closed loop dividers and a final output multiplexer to achieve the desired dividing ratios for the clock output.

The accuracy of the frequencies produced by the ST49C106 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLKO = (Reference clock) X A/(B.C)

where A=1,2,3,......127 B=8, 16, 32,64 C=1,2,4,8

For proper output frequency, the ST49C106 can accept a reference frequency from 5 - 40 MHz and divider ratio up to 15.

ABSOLUTE MAXIMUM RATINGS

Supply range Abole benefit as been to need the at CLATX Voltage at any pin

Operating temperature

Storage temperature

Package dissipation TAH need W (NAC) below level abole

7 Volts GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

DC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
VIL	Input low level + eleni2 sosilov	Analog supply		0.8	VS	22)
V _{IL} V _{IH}	Input high level	2.0			V	
V _{OL}	Output low level Output high level	2.4		0.4	V	I _{oL} = 8.0 mA
I _{IL}	Input low current	2.4		-350	μА	I _{OH} = 8.0 mA Except crystal
I _{IH}	Input high current			1	μА	input V _{IN} =Vcc
I _{cc}	Operating current		20	30	mA	No load. DCLK=80MHz
R _{IN}	Input pull-up resistance	15	20	25	ΚΩ	DOLIN JOHN IZ

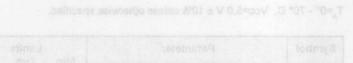
AC ELECTRICAL CHARACTERISTICS

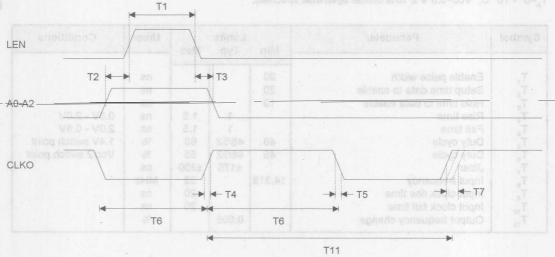
 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

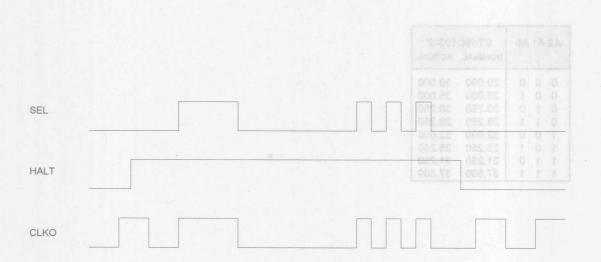
Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
T ₁	Enable pulse width	20	ETE	- p-	ns	pd P
T ₂	Setup time data to enable	20			ns	
T,	Hold time to data enable	10	7		ns	
T ₃	Rise time		1_	1.5	ns	0.8V - 2.0V
T,	Fall time		1.	1.5	ns	2.0V - 0.8V
T ₅ T ₆ T ₆	Duty cycle	40	48/52	60	%	1.4V switch point
T ₆	Duty cycle	45	48/52	55	%	Vcc/2 switch point
T ₇	Jitter		±175	±300	ps	
T ₈ T ₉	Input frequency	14.318		32	MHz	
T.	Input clock rise time		A-10	20	ns	*
T ₁₀	Input clock fall time			20	ns	
T ₁₁	Output frequency change	87	0.005		%	

A2	A1	A0	ST49C106-5*					
0	0	0	39.000	39.000				
0	0	1	25.000	25.000				
0	1	0	30.750	30.750				
0	1	1	26.250	26.250				
1	0	0	32.000	32.000				
1	0	1	25.250	25.250				
1	1	0	31.250	31.250				
1	1	1	37.500	37.500				











ST49C107

Printed September 2, 1994

PREPROGRAMMED CPU MOTHER BOARD FREQUENCY GENERATOR

DESCRIPTION

The ST49C107 is a mask programmable monolithic analog CMOS device designed to generate two similtaneous clock. One clock, the BCLK (buffered reference clock), is a fixed output frequency. The other clock, CLOCK, 1XCLK, and 2XCLK can vary from 2 to 100MHz, with up to 16 single selectable preprogrammed frequencies stored in internal ROM. The ST49C107 is designed to replace existing CPU mother board clocks generated from individual oscillators in order to reduce board space and number of oscillators. To provide high speed and low jitter clock, the parts utilize a high speed analog CMOS phase locked loop using 14.318 MHz system clock as the reference clock (note that reference clock can be changed to generate optional frequencies from a standard programmed device). The programmed clock outputs are selectable via four address lines (two address lines for ST49C107-05).

FEATURES

- · Provides reference clock and synthesized clock
- 5 to 40MHz input reference frequency
- Pin-to-pin compatible to Avasem AV9107
- Programmable analog phase locked loop
- Low power single 5V CMOS technology
- Up to 16 frequencies stored internally
- 8/14 pin DIP or SOIC package.

SOIC Package

A1 1	2.20,76 val 1146 vision (46.71 (46.00)	14	AO
A2 2	4	13	BCLK
A3 3	CF1	12	VCC
AGND 4	2107	11	CLOCI
DGND 5	490	10	CE2
PD* 6	ST	9	OE1
XTAL1 7	- Long	8	XTAL2

ST49C107CF-03

A1 1		14	A0
A2 2	4	13	1XCLK
A3 3	07CF14	12	VCC
AGND 4	_	11	2XCLK
DGND 5	49C	10	CE2
PD* 6	ST	9	OE1
XTAL1 7		8	XTAL2

ST49C107CF-04

ORDERING INFORMATION

 Part number
 Package
 Operating temperature

 ST49C107CP8
 Plastic-DIP
 0 ° C to +70° C

 ST49C107CF8
 SOIC
 0° C to +70° C

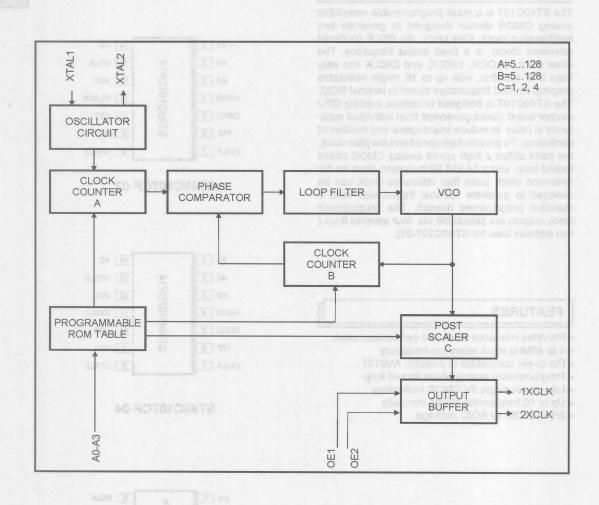
 ST49C107CP14
 Plastic-DIP
 0 ° C to +70° C

 ST49C107CF14
 SOIC
 0° C to +70° C

A0 1	1 8	8 BCLK
GND 2	07CF	7 VCC
XTAL1 3	49C1	6 CLOCK
XTAL2 4	- I	5 A1

ST49C107CF-05

BLOCK DIAGRAM



Symbol	Pin	Signal Type	Pin Description
A1	1* 5 Jugo	select liddress	Frequency select address input 2.
A2	2*	select hodress	Frequency select address input 3.
A3	3*	select leddress	Frequency select address input 4.
AGND	4	ound, O	Analog ground.
DGND	5	o und.	Digital ground.
PD wol sen	w tuilo 6* sturi8	wn (Actifre low).	Power-Down (Active low). Shuts off chip when low.
u phase inched 8 MHz oleur,			
XTAL2	8	O Jug	Crystal output.
OE1		COutpulEnable ited when this p	Buffered clock Output Enable (Active high). BCLK output is three stated when this pin is low.
OE2 MOOLO		CuroulEnable	Clock Output Enable (Active high). CLOCK output is three stated when this pin is low.
CLOCK	11	zhola (Ortua be	Programmed output clock.
vcc	atto12 + bign	ipply veltage. St	Positive supply voltage. Single +5 volts.
BCLK	13. Jugiuo	C Divid Oby-two	Buffered crystal clock output.
Α0	14*, hugh	select Induces	Frequency select address input 1.

^{*} Have internal pull-up resistors on inputs.

SYMBOL DESCRIPTION (ST49C107-04 package) NO TO TO TO THE MONTH NO THE

Symbol	Pin	Signal Type	Pin Description
A1	1* \$ Juqu	select Iddress	Frequency select address input 2.
A2	2* Jugn	select Indiress	Frequency select address input 3.
A3	3*	select Indiress	Frequency select address input 4.
AGND	4	o .biui	Analog ground.
DGND	5	O bras	Digital ground.
PD wol ned	w qirlo 6* ahrifa	vn (Active low).	Power-Down (Active low). Shuts off chip when low.
			Crystal or EXternal Clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	8	O hug	Crystal output. 6 8 SJATX
OE1 007U08		ock Ou l put Enal d when this pin	
OE2) a lugino	00.110*lpid s	out Enake (Active this pin is low	2X-CLOCK Output Enable (Active high). 2X-CLOCK output is three stated when this pin is low.
2XCLK	11	ed out Ot clock	Programmed output clock.
vcc	allo12 + slow	ipply veltage, Si	Positive supply voltage. Single +5 volts.
1XCLK	13	ystat cock outp	2X-CLOCK Divide-by-two output.
A0	14*	adenti Indonésa	Frequency select address input 1.

^{*} Have internal pull-up resistors on inputs.

Symbol	Pin	Signal Type	Pin Description
A0	1		Frequency select address input 1.
A1	5	1	Frequency select address input 2.
GND	2	0	Supply ground.
XTAL1	3	1	Crystal or EXternal Clock input. A crystal can be connected
Conditions		Limits Typ Max	to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock XTAL2 is left open or used as buffered clock output.
XTAL2	4	0	Crystal output.
CLOCK	6	4.0 o	Programmed output clock.
vcc	7	10	Positive supply voltage. Single +5 volts.
BCLK	8	20 0 30	Buffered crystal clock output.

FREQUENCY TRANSITIONS

The ST49C107 is designed to provide smooth, glitch-free frequency transitions on the CLOCK, 1XCLK and 2XCLK clocks when the frequency select pins are changed. These frequency transitions are less than 0.1% frequency change per clock period.

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect 0.047 μ F capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C107 contains an analog phase locked loop circuit with digital closed loop dividers and a final output multiplexer to achieve the desired dividing ratios for the clock output.

The accuracy of the frequencies produced by the ST49C107 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLOCK = (Reference clock) X A/(B.C)

where A=5, 6, 7,......128 B=5, 6, 7,.....128 C=1,2

For proper output frequency, the ST49C107 can accept a reference frequency from 5 - 40 MHz and divider ratio up to 15.

ABSOLUTE MAXIMUM RATINGS

Supply range 7 Volts
Voltage at any pin GND-0.3 V to VCC+0.3 V
Operating temperature 0° C to +70° C
Storage temperature -40° C to +150° C
Package dissipation 500 mW

DC ELECTRICAL CHARACTERISTICS

 $T_A = 0^{\circ} - 70^{\circ} C$, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
V _{IL}	Input low level Input high level	2.0		0.8	V	CTAL2
V _{OL}	Output low level Output high level	2.4		0.4	V	I _{OL} = 8.0 mA I _{OH} = 8.0 mA
I _{IL}	Input low current Input high current	Positive su	1	-10 1	μA μA	Exc. crystal input
I _{cc}	Operating current	Buffered or	20	30	mA ₈	No load. CLOCK=80MHz
I _{SB}	Standby current Input pull-up resistance	500	25 900	1300	μΑ ΚΩ	No load.

AC ELECTRICAL CHARACTERISTICS

 $T_{\Delta}=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
<u>T</u> ,	1X, 2X-CLOCK rise time	la la	ba q mm	1.5	ns	0.8V - 2.0V
T ₂	1X, 2X-CLOCK fall time	40	1 48/52	1.5	ns %	2.0V - 0.8V 1.4V switch point
T ₅	Duty cycle	45	48/52	55	%	Vcc/2 switch point
T ₃	Jitter 3 3 3 3 3 3		±175	±300	ps	
T	Input frequency	2		32	MHz	
T ₇	Buffered clock rise time			20	ns	
T ₈	Buffered clock fall time			20	ns	
T ₆ M O	1X, 2X-CLOCK frequency change		0.005		%	

CLOCK OUTPUT TABLE FOR ST49C107-03 (using 14.318 MHz input. All frequencies in MHz).

CLOCK OUTPUT TABLE FOR ST49C107-05 (using 14.318 MHz input. All frequencies in MHz).

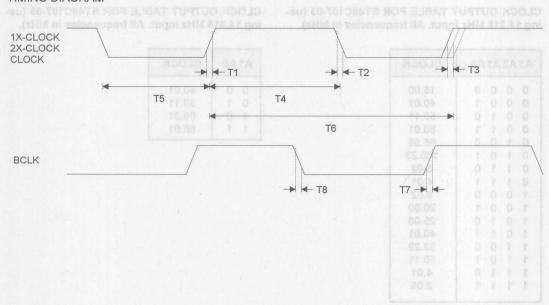
A3	A2	A1	A0	CLOCK
0	0	0	0	16.00
0	0	0	1	40.01
0	0	1	0	50.11
0	0	1	1	80.01
0	1	0	0	66.58
0	1	0	1	100.23
0	1	1	0	8.02
0	1	1	1	4.01
1	0	0	0	8.02
1	0	0	1	20.00
1	0	1	0	25.06
1	0	1	1	40.01
1	1	0	0	33.29
1	1	0	1	50.11
1	1	1	0	4.01
1	1	1	1	2.05

A1 A0	CLOCK
0 0	40.01
0 1	50.11
1 0	66.61
1 1	80.01

CLOCK OUTPUT TABLE FOR ST49C107-04 (using 14.318 MHz input. All frequencies in MHz).

А3	A2	A1	A0	2X-CLOCK	CLOCK
0	0	0	0	80.02	40.01
0	0	0	1	66.62	33.31
0	0	1	0	50.11	25.06
0	0	1	1	40.01	20.00
0	1	0	0	100.23	50.11
0	1	0	1	33.31	16.66
0	1	1	0	32.01	16.00
0	1	1	1	25.06	12.47
1	0	0	0	64.02	32.01
1	0	0	1	2X-Input	1X-Input
1	0	1	0	3X-Input	1.5X-Input
1	0	1	1	8X-Input	4X-Input
1	1	0	0	0.5X-Input	0.25X-Input
1	1	0	1	0.25X-Input	0.125X-Input
1	1	1	0	120.00	60.00
1	1	1	1	129.96	64.98

TIMING DIAGRAM



CLOCK OUTPUT TABLE FOR STANCIOTO4 (us ing 14.318 MHz Input. All frequencies in MHz).



ST49C154

Printed September 2, 1994

PREPROGRAMMED CPU MOTHERBOARD FREQUENCY GENERATOR

GENERAL DESCRIPTION

The ST49C154 is a monolithic analog CMOS device designed to generate six simultaneous clock outputs for mother board and disk drive applications. It is designed in a 1.2μ process to achieve 100 MHz operation with low clock jitter.

The ST49C154 may be used to replace existing BUS, I/O, and disk drive clocks generated from individual oscillators so that board space and number of oscillators are reduced. The high speed analog CMOS phase locked loops use the 14.318 MHz system clock or external crystal connected between XTAL1 and XTAL2 as the reference clock (reference clock can be changed to generate non-standard frequencies from the standard programmed device).

The ST49C154 is metal mask programmable to provide any custom set of CPUCLK frequencies. The programmed clock outputs are selectable via four address lines for 1XCLK / 2XCLK outputs. The CPU clock makes glitch-free transitions from one frequency to the next and follows Intel's processors input clock specification.

FEATURES

- Pin -to-pin compatible to AV9154
- · Compatible with 286, 386, and 486 CPUs
- Supports Turbo modes
- Generates communications clock, keyboard clock, floppy disk clock, system reference clock, bus clock and CPU clock
- Skew controlled 2X and 1X clocks
- Programmable analog phase locked loop
- High speed (up to 130 MHz output)
- Low power single 3V / 5V CMOS technology
- 16 pin dip or SOIC package

ORDERING INFORMATION

Part number	Package	Oper	atin	g te	mperati	ure
ST49C154CP16-xx	Plastic-DIP	0°	C	to	+70°	C
ST49C154CF16-YY	SOIC	O°	C	to	+70°	C

SOIC Package

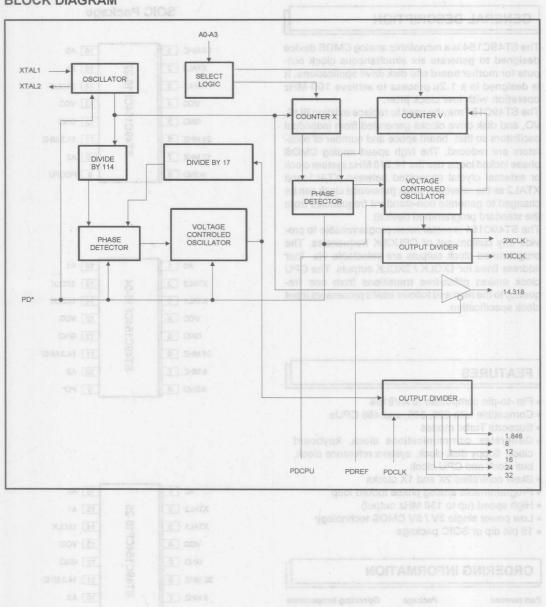
1.8 MHZ	1	16 A0
XTAL2	2 2	15 A1
XTAL1	2 3 4 19-51	14 2XCLK
VCC	4 04	13 VCC
GND	5 5	12 GND
24 MHZ	ST49C154C	11 14.3 MHZ
12 MHZ	7 · · · · ·	10 A2
AGND [8	9 PDCPU

A0 1		16 A1
XTAL2 2	40	15 2XCLK
XTAL1 3	-91	14 1XCLK
VCC 4	ST49C154CF16-04	13 VCC
GND 5	C15	12 GND
24 MHZ 6	L49	11 14.3 MHZ
8 MHZ 7	S	10 A2
AGND 8		9 PD*

A2 1	in many to a sumprior resident	16 A0
XTAL2 2	.25	15 A1
XTAL1 3	54CF16-25	14 1XCLK
VCC 4	4CF	13 VCC
GND 5	C15	12 GND
32 MHZ 6	ST49C1	11 14.3 MHZ
8 MHZ 7	လ	10 A3
AGND 8	* '	9 PD*

1

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
XTAL2		CPU Odkovana	Crystal output.
XTAL1	3	-4, -5, -6, -10 -16 1	Crystal or External clock input.
VCC	4,13	1-4, -6, -10 > pin 1	Digital supply voltage. Single +3 / +5 volts.
GND	5,12	0 PM 14	Digital signal ground.
AGND	8	c check output.	Analog ground.
A0	*	-4, -5 -25 > pm A	CPU clock frequency select address 0. ST49C154-4, -6, -16, -26, -60 > pin 1. ST49C154-5, -10, -25, -27 > pin 16.
A1	*		CPU clock frequency select address 1. ST49C154-4, -6, -16, -26, -60 > pin 16. ST49C154-5, -10, -25, -27 > pin 15.
A2	Sutent. -27, -63 > ph	-4, -5, -6, -18, -25 -10 > pin 1G.	ST49C154-5, -25 > pin 1. ST49C154-6, -16, -60 > pin 15.
А3	*	bok output. -5101 pin 6.	CPU clock frequency select address 3. ST49C154-5, -25 > pin 10.
PD*	76C*> pin 6.	ock cutput. -4 -6, -1 16 -26 -2 -10 > pin 11	Power down (active low). Shuts off entire chip when low. ST49C154-4, -5, -25, -26 > pin 9.
PDCPU	*	ock out, but. -26 > pin 6.	Power down (active high). Shuts off 2XCLK output when high. ST49C154-6, -16, -60 > pin 10.
PDREF	*	lock output. I-6, -60 I- pin 7.	Power down (active high). Shuts off the 14.318 MHz reference clock output. ST49C154-6, -16, -60 > pin 9.
PDCLK*	*	1	Power down (active low). Shuts off the 1.846 MHz, 8 MHz, 16 MHz, and 24 MHz clock outputs. ST49C154-10 > pin 9.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description	
1XCLK	*	O dugi	Selectable CPU clock output. ST49C154-4, -5, -6, -10, -16, -25, -60 > pin 14.	XTAL2
4		External clock in	10 leien 3	
2XCLK	*	0	Selectable 2X-CPU clock output.	
2		ply voltage. Singl	ST49C154-4, -6, -60 > pin 15. ST49C154-27 > pin 14.	
		tat ground.		
1.846 MHz	*	O bine	1.846 MHz clock output. ST49C154-10 > pin 7.	
		frequency select	ST49C154-27 > pin 1.	
8 MHz	.f r ti q ≤ 0 ,at niq	-4, -6, 0 6, -26, -8 -5, -10, -26, -27	8 MHz clock output. ST49C154-4, -5, -25 > pin 7. ST49C154-10 > pin 1.	
		frequency select	ladio USO I CPU closi	
12 MHz		-4, -8, 0 6, -26, -8 -5, -10, -25, -27	12 MHz clock output. ST49C154-16, -26, -27 > pin 7.	
14.318 MHz		frequeOcy select -4, -26, -27 > pin -5, -25 > pin 1, -6, -16, -60 > pin	14.318 MHz reference clock output. ST49C154-4, -5, -6, -16, -25, -27, -60 > pin 11. ST49C154-10 > pin 10.	
16 MHz	*	nequency select	16 MHz clock output. ST49C154-5, -10 > pin 6.	
24 MHz	* Shuts off entire	0	24 MHz clock output. ST49C154-4, -6, -16, -26, -27, -60 > pin 6.	
32 MHz		(rigin = 0 los) nv	32 MHz clock output. ST49C154-25 > pin 6.	
128 kHz	*	O muid evitos) ma	128 kHz clock output. ST49C154-6, -60 > pin 7.	

SYMBOL DESCRIPTION (ST49C154-22 with 25 MHz reference frequency)

Symbol	Pin	Signal Type	Pin Description	
XTAL2	2	0	Crystal output.	
XTAL1	\$8.9	31 715	Crystal or External clock input.	
VCC	3,10,13	16.11 160 1 20.05 40	Digital supply voltage, Single +3 / +5 volts.	
GND	4,12	26 0 50	Digital signal ground.	
AGND	7.	08 00.04 10 00.03	Analog ground.	
20 MHz	15	0	20 MHz clock output.	
24 MHz	5	32.26	24 MHz clock output.	
25 MHz	11	0	25 MHz clock output.	
32 MHz	6	0 08	32 MHz clock output.	
40 MHz	14	0	40 MHz clock output.	
	Resident or	101 1010 10	asset on a law at arrive	

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ST49C154 ACTUAL OUTPUT FREQUENCIES (using 14.318 MHz input. All frequencies in MHz).

lodenye	CLK -60	CLK -27	CLK -25	CLK -16	CLK -10	CLK -6	CLK -5	A0	A1	A2
	- 00	21	20							
	8.182	75.17	2.15	16.11	PDCPU	16.11	2.15	0	0	0
	16.11	31.94	8.18	20.05	40.09	20.05	8.18	1	0	0
	20.05	60.136*	16.11	25.06	50.11	25.06	16.11	0	1	0
	25.06	40.09	20.05	33.41	66.48*	33.24	20.05	1	1	0
	33.24	50.11	25.06	40.09	iono tempi	40.09	25.06	0	0	1
	40.09	66.48*	33.24	50.11	availy instilled	50.11	33.24	1	0	1
	50.11	80.18*	40.09	66.48*	greund.	66.48	40.09	0	1	1
	66.48*	51.90	50.11	80.18*	ground.	80.18*	50.11	1	1	1
	15		4.30	elita ne	clock outg		4.30	0	0	0
	-		16.11		duen vincino		16.11	1	0	0
	5		32.22		plack outp	100	32.22	0	1	0
			40.09		grace mineral		40.09	1	1	0
	11		50.11		elock outs	200	50.11	0	0	1
		1	66.48*				66.48*	1	0	1
	. 9		80.18*		the dock		80.18*	0	1	1
			100.23*				100.23*	1	1	1
	0.128	1.846	8.00	12.00	1.846	0.128	8.00	11441		1/0
	14.318	12.00	14.318	14.318	8.00	14.318	14.318		10	loc
	24.00	14.318	32.01	24.00	14.318	24.00	16.00		13	100
	24.00	24.00	32.01	24.00	16.00	24.00	10.00			
		24.00	2		S. 4245 (2) (2)				4.	
	- T				24.00			- In		

ST49C154-04, -26 ACTUAL OUTPUT FREQUENCIES (using 14.318 MHz input. All frequencies in MHz).

A2 A1 A0		2 A1 A0 2XCLK		1XCLK	
0	0	0	100.23*	50.11	
0	0	1	80.18*	40.09	
0	1	0	66.48*	33.24	
0	1	1	50.11	25.06	
1	0	0	40.09	20.05	
1	0	1	32.22	16.11	
1	1	0	24.23	12.12	
1	1	1	15.75	7.88	
	1/0		8.00,	12.00**	
Clocks		ks	24.00		
			14.318		

XTAL2 1		16 N.C.
XTAL1 2	16-22	15 20 MHZ
VCC 3	-16-	14 40 MHZ
GND 4	54CF1	13 VCC
24 MHZ 5	215	12 GND
32 kHZ 6	ST49C1	11 25 MHZ
AGND 7	, o	10 VCC
N.C. 8		9 N.C.

^{*}These selections will only operate at 5V.

^{**} ST49C154-26 only

ABSOLUTE MAXIMUM RATINGS

Supply voltage
Voltage at any pin
Operating temperature
Storage temperature
Package dissipation

7 Volts GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

DC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parame	Min	Limits Min Typ		Units	Conditions	
V _{IL} V _{IH} V _{OL} V _{OH} I _{IL} I _{IH} I _{CC} I _{SB} I _{SC} CC CC	The second secon	100 ±2.00 ±2	2.0 2.4	25 15 40 10 20	0.8 0.4 -5 5 40	V V V Д Д Д Д Д Д Д Д Д Д Д Д Д Д Д Д Д	I _{oL} = 4.0 mA I _{oH} = -8.0 mA V _{IN} =0V V _{IN} =Vcc No load. Power down. Each output clock Except Xtal1,2

A2 1 16 A0 XTAL2 2 ST49C154CF16-05 15 A1 XTAL1 3 14 1XCLK VCC 4 13 VCC GND 5 12 GND 16 MHZ 6 11 14.3 MHZ 8 MHZ 7 10 A3 AGND 8 9 PD*

16 A1 A0 1 XTAL2 2 ST49C154CF16-06 15 A2 XTAL1 3 14 1XCLK VCC 4 13 VCC GND 5 12 GND 24 MHZ 6 11 14.3 MHZ 128 kHZ 7 10 PDCPU AGND 8 9 PD*

AC ELECTRICAL CHARACTERISTICS

 $T_A = 0^{\circ} - 70^{\circ} \text{ C}$, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter			Limits Typ	Max	Units	Conditions	
T ₄	Rise time 0.8 to 2.0V			1	2	ns	15pF load	
T,	Fall time 0.8 to 2.0V			80118	2	ns	15pF load	
T.	Duty cycle		40	48/52	60	%	15pF load	
T _p	Reference clock duty cycle	bei	40	48/52	55	% / 0	=0" - 70" C. Voce5	
T_5 T_6 T_R T_T	Frequency transition time				20	ms	From 2-20MHz	
T _P	Power up time			15		ms	From off to 50MHz	
Tenoiti	Output frequency		2		50	MHz	iodiny2	
-T,	Input frequency	mi	2	14.318	32	MHz		
T _{IF}	Input clock rise/fall time	-			20	ns		
T,	Jitter V 8.0			±175	±300	ps	16-100MHz	
Tus	Jitter, 1 sigma	- 0		±0.8	±2.5	%	All frequencies	
I JA	Jitter, absolute			2	5	%	All frequencies	
T ₈ Am	Input frequency	4	2	14.318	32	MHz	rt Bright O IIIV	
T ₈ T ₉ T ₁₀	Input clock rise time				20	ns	wel lugat	
T ₁₀	Input clock fall time				20	ns	igin/suont Inout/higi	
TE	Enable pulse width		20		Mar.	ns	l _{cc} Operating	
Ts	Clock skew berween 1XCLK			0.5	1.0	ns	(g) Stand by	
put clock	and 2XCLK	6				nemup liu	ale hori2 short cla	
						sonstion	C. Input cap	

8 MHZ 1		16 A0	A0 1	16 A1
XTAL2 2	9	15 A1	XTAL2 2	9 15 A2
XTAL1 3	16	14 1XCLK	XTAL1 3	9 14 1XCLK
VCC 4	4CF	13 VCC	VCC 4	O 13 VCC
GND 5	215	12 GND	GND 5	12 GND
16 MHZ 6	ST49C154CF16-10	11 24 MHZ	24 MHZ 6	12 GND 11 14.3 MH
1.8 MHZ 7	S	10 14.3 MHZ	12 MHZ 7	O 10 PDCPU
AGND 8		9 PDCLK*	AGND 8	9 PDREF

16 A1
15 A2
14 1XCLK
13 VCC
12 GND
11 14.3 MHZ
10 PDCPU
9 PD*

1

ABSOLUTE MAXIMUM RATINGS

Supply voltage

Voltage at any pin

Operating temperature

Storage temperature

Package dissipation

Voltage seawand assign of the following sealing sealing of the following sealing sea

DC ELECTRICAL CHARACTERISTICS

 $T_{\Delta}=0^{\circ}$ - 70° C, Vcc=3.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Min Typ Max			Conditions	
V _{IL}	Input low level	0.7VCC		0.15VCC	V	e iew. da will.	
V _{OL} V _{OH}	Output low level			0.1	V	I _{OL} = 8.0 mA	
V _{OH}	Output nigh level	VCC-0.1V			V	$I_{OH}^{OE} = -4.0 \text{ mA}$	
I _{IL}	Input low current	-5		-5	μΑ	V _{IN} =0	
I _{IH}	Input high current	-5		5	μА	V _{IN} =Vcc	
Icc	Operating current		15		mA	No load.	
I _{SB}	Stand by current		15		μΑ	Power down.	
1	Short circuit current		15		mA	No load.	
C _I	Input capacitance	-		10	pF	Except Xtal1,2	
C,	Load capacitance		30		pF		

A0 1		16 A1	A0 1	
XTAL2 2	-56	15 2XCLK	XTAL2 2	09
XTAL1 3	CF16-26	14 1XCLK	XTAL1 3	CF16-60
VCC 4	54CF	13 VCC	VCC 4	ļ
GND 5	C15	12 GND	GND 5	ST49C154
24 MHZ 6	ST49C1	11 14.3 MHZ	24 MHZ 6	149
12 MHZ 7	, v	10 A2	128 kHZ 7	, v
AGND 8		9 PD*	AGND 8	

AC ELECTRICAL CHARACTERISTICS

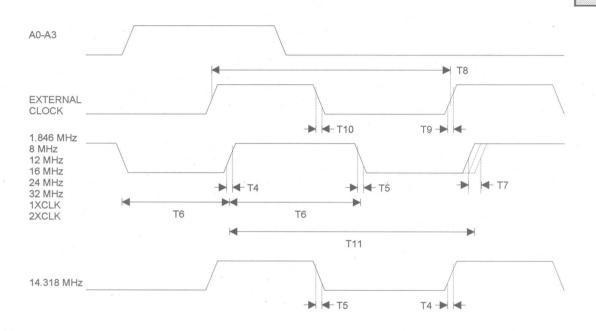
 $T_A=0^{\circ}$ - 70° C, Vcc=3.0 V ± 10% unless otherwise specified.

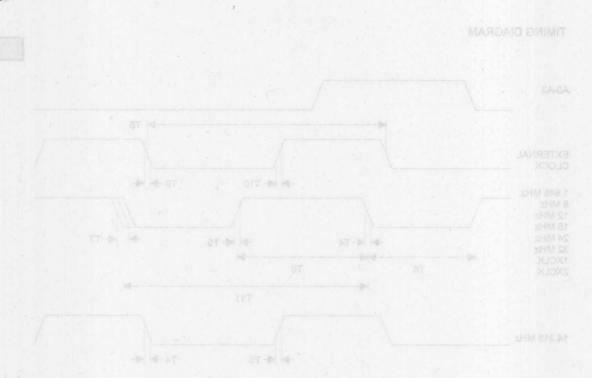
Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
T ₄ T ₅ T ₆ T ₇	Rise time Fall time Duty cycle Frequency transition time	40	48/52	4 4 60 20	ns ns % ms	15pF load. 15pF load. 15pF load. From 2-20MHz
T _P	Power up time Output frequency	balloaga a	15	50	ms MHz	From off to 50MHz
T ₈	Input frequency Input clock rise/fall time	2	14.318	32 20	MHz ns	Symbol
T ₇ T _{JIS} T _{JA} T ₉ T ₁₀ T _E	Jitter Jitter, 1 sigma Jitter, absolute Input clock rise time Input clock fall time Enable pulse width	20	±175 ±8.5 ±3	±300 ±2 ±5 20 20	ps % % ns ns ns	All frequencies All frequencies
	15 mA No load. 16 pA Power do 15 nA No load. 16 nA No load.					loc Operating



TIMING DIAGRAM

1







ST49C155

Printed September 12, 1994

PREPROGRAMMED CPU MOTHERBOARD FREQUENCY GENERATOR

GENERAL DESCRIPTION

The ST49C155 is a monolithic analog CMOS device designed to generate eight simultaneous clock outputs for mother board applications. It is designed in a 1.2μ process to achieve 130 MHz operation with low clock jitter.

The ST49C155 may be used to replace existing BUS and I/O clocks generated from individual oscillators so that board space and number of oscillators are reduced. The high speed analog CMOS phase locked loops use the 14.318 MHz system clock or external crystal connected between XTAL1 and XTAL2 as the reference clock (reference clock can be changed to generate non-standard frequencies from the standard programmed device).

The ST49C155 is metal mask programmable to provide any custom set of CPUCLK frequencies. The programmed clock outputs are selectable via four address lines for 1XCLK / 2XCLK outputs.

SOIC Package

CLK1 1		20	AO
XTAL2 2	1	19	A1
XTAL1 3	- 2	18	1XCL
DVCC 4	20-0	17	2XCL
DGND 5	ST49C155CF20-01 ST49C155CF20-02	16	AVC
CLK2 6	49C1	15	AGNI
CLK3 7	STS	14	CLK
CLK4 8		13	CLK
AGND 9		12	PD*
OE . 10		11	A2
	-	4	

FEATURES

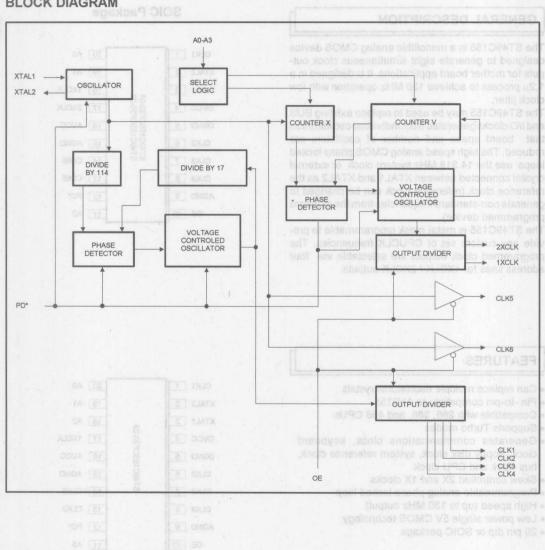
- · Can replace multiple oscillators/crystals
- Pin -to-pin compatible to AV9155
- · Compatible with 286, 386, and 486 CPUs
- Supports Turbo modes
- Generates communications clock, keyboard clock, floppy disk clock, system reference clock, bus clock and CPU clock
- Skew controlled 2X and 1X clocks
- Programmable analog phase locked loop
- High speed (up to 130 MHz output)
- Low power single 5V CMOS technology
- 20 pin dip or SOIC package

ORDERING INFORMATION

Part number	Package	Oper	atin	g te	mperati	ure
ST49C155CP20-xx	Plastic-DIP	0°	C	to	+70°	C
ST49C155CF20-xx	SOIC	0°	C	to	+70°	C
ST49C155CJ20-xx	PLCC	0°	C	to	+70°	C

CLK1 1		20	A0
XTAL2 2		19	A1
XTAL1 3	e e	18	A2
DVCC 4	ST49C155CF20-23	17	1XCLK
DGND 5	55CF	16	AVCC
CLK2 6	49C1	15	AGND
CLK3 7	ST	14	CLK6
CLK4 8		13	CLK5
AGND 9		12	PD*
OE 10		11	АЗ

BLOCK DIAGRAM



SYMBOL DESCRIPTION (ST49C155-01/ -02) (80-88108818) MORESTROZER AND RESERVED AND

Symbol	Pin	Signal Type	Pin Description
CLK1	1	outpuo e	1.8432 MHz clock output.
XTAL2	2	0 10	Crystal output.
XTAL1	3	stemat block input	Crystal or External clock input.
DVCC	64 v 8	ly voltabe. Single	Digital supply voltage. Single +5 volts.
DGND	5	.1Opong 1g	Digital signal ground.
CLK2	6	ppy disk O .tock ou p	16 MHz (ST49C155-01) or 32 MHz (ST49C155-02) clock output.
CLK3	7	dugline kaolo e	24 MHz floppy disk clock output.
CLK4	8	oard clock output.	12 MHz keyboard clock output.
AGND	9	0	Analog ground.
OE .	10*	ble (aclive high) wee 340s mode	Output Enable (active high). Low on this pin sets all the outputs to three state mode.
A2	11	nednesich seiter Bi	CPU clock frequency select address 2.
PD*	12*	t (active low). Sin	Power down (active low). Shuts off entire chip when low.
CLK5	13	0	14.318 MHz reference clock output.
CLK6	14	0	14.318 MHz reference clock output.
AGND	15	al ground.	Analog ground.
AVCC	16	1	Analog supply voltage. Single +5 volts.
2XCLK	17	- Indiad	2X CPU clock output.
1XCLK	18	l I	1X CPU clock output.
A1	19	1	CPU clock frequency select address 1.
A0	.0 aas ibb	requercy selecting	CPU clock frequency select address 0.

^{*}Have internal pull-up resistor on inputs

SYMBOL DESCRIPTION (ST49C155-03)

Symbol	Pin	Signal Type	Pin Description	
CLK1	1	clock o fput.	6 MHz clock output.	7(1)
XTAL2	2	0 10	Crystal output.	
XTAL1	3	Memal block input	Crystal or External clock input.	
DVCC	4	ly voltate, Single	Digital supply voltage. Single +5 volts.	
DGND	5	louge to	Digital signal ground.	
CLK2 30-88	DENTS 6 THE	149C19OUT) or 22	24 MHz floppy disk clock output.	
CLK3	7	0	16 MHz bus clock output.	
CLK4	8	o O O O O O O O O O O O O O O O O O O O	8 MHz keyboard clock output.	
AGND	9	no será clock euty un	Analog ground.	
OE of the stee no	10*	o O ble (active Nigh), I	Output Enable (active high). Low on this pin sets all outputs to three state mode.	the
A3	11	Leboni siais esni	CPU clock frequency select address 3.	
PD*	12*	1	Power down (active low). Shuts off entire chip when le	ow.
CLK5	13	O (WOLEVERS)	14.318 MHz reference clock output.	
CLK6	14	0	14.318 MHz reference clock output.	
AGND	15	0	Analog signal ground.	
AVCC	16	I J	Analog supply voltage. Single +5 volts.	
1XCLK	17	aly voltage. Single	CPU clock output.	
A2	18	ck output.	CPU clock frequency select address 2.	
A1	19	ck output	CPU clock frequency select address 1.	
A0	20	requency select at	CPU clock frequency select address 0.	

^{*}Have internal pull-up resistor on inputs

CPU CLOCK TABLE FOR ST49C155-01, -02 (using 14.318 MHz input. All frequencies in MHz).

	1XCLK	2XCLK	A0	A1	A2
0	4	8	0	0	0
Ó.	8	16	1	0	0
1	16	32	0	1	0
0	20	40	1	1	0
1	25	50	0	0	1
0	33.33	66.66	1	0	1
	40	80	0	1	1
-	50	100	1	1	1

CPU CLOCK TABLE FOR ST49C155-03(using 14.318 MHz input. All frequencies in MHz).

	1XCLK	١0	A1	A2	А3
	16	0	0	0	0
	40	1	0	0	0
	50	0	14	0	0
	80	1	1	0	0
	66.66	0	0	1	0
	100	1	0	1	0
	8	0	1	1	0
	4	1	1	1	0
	8	0	0	0	1
	20	1	0	0	1
	25	0	1	0	1
	40	1 🖪	1	0	1
	33.33	0	0	1	1
	50	1	0	1	1
	4	0	1	1	1
	2	1	1	1	1

CPU CLOCK TABLE FOR ST49C155-23(using 14.318 MHz input. All frequencies in MHz).

A2	A2 A1 A0		A1 A0 2XCLK		1XCLK	
0	0	0	75	37.5		
0	0	1	32	16		
0	1	0	60	30		
0	1	1	40	20		
1	0	0	50	25		
1	0	10	66.66	33.33		
1	1	0	80	40		
1	1	1	52	26		

PERIPHERAL CLOCK TABLE CHART FOR ST49C155-01 (MHz)

CLK1	CLK2	CLK3	CLK4
1.8432	16	24	12

PERIPHERAL CLOCK TABLE CHART FOR ST49C155-02 (MHz)

CLK1	CLK2	CLK3	CLK4
1.8432	32	24	12

PERIPHERAL CLOCK TABLE CHART FOR ST49C155-03 (MHz)

CLK1	CLK2	CLK3	CLK4
6	24	16	8

PERIPHERAL CLOCK TABLE CHART FOR ST49C155-23 (MHz)

CLK1	CLK2	CLK3	CLK4
1.843	16	24	12

ACTUAL OUTPUT FREQUENCIES

CPU CLOCK TABLE FOR ST49C155-01, -02 (using 14.318 MHz input. All frequencies in MHz).

A2	A2 A1 A0		A2 A1 A0 2XCLF		2XCLK	1XCLK
0	0	0	7.5	3.75		
0	0	1	15.51	7.76		
0	1	0	32.22	16.11		
0	1	1.	40.09	20.05		
1	0	0	50.11	25.06		
1	0	1	66.82	33.41		
1	1	0	80.18	40.09		
1	1	1	100.23	50.11		

CPU CLOCK TABLE FOR ST49C155-03(using 14.318 MHz input. All frequencies in MHz).

А3	A2	A1	A0	1XCLK
0	0	0	0	15.51
0	0	0	1	40.09
0	0	1	0	50.11
0	0	1	1	80.18
0	1	0	0	66.82
0	1	0	1	100.23
0	1	1	0	7.58
0	1	1	18	4.30
1	0	0	0	7.76
1	0	0	1	20.05
1	0	1	0	25.06
1	0	1	1	40.09
1	1	0	0	33.41
1	1	0	1	50.11
1	1	1	0	3.79
1	1	1	1	2.15

CPU CLOCK TABLE FOR ST49C155-23(using 14.318 MHz input. All frequencies in MHz).

A2 A1 A0		2XCLK	1XCLK
0 0	0	75.170	37.585
0 0	1	31.940	15.970
0 1	0	60.136	30.068
0 1	1	40.090	20.045
1 0	0	50.113	25.057
1 0	1	66.476	33.238
1 1	0	80.181	40.091
1 1	1	51.903	25.952

PERIPHERAL CLOCK TABLE CHART FOR ST49C155-01 (MHz)

CLK1	CLK2	CLK3	CLK4	
1.8432	16	23.71	11.86	

PERIPHERAL CLOCK TABLE CHART FOR ST49C155-02 (MHz)

CLK1	CLK2	CLK3	CLK4
1.8432	32.01	24	12

PERIPHERAL CLOCK TABLE CHART FOR ST49C155-03 (MHz)

CLK1	CLK2	CLK3	CLK4	
6	24	16	8	

ABSOLUTE MAXIMUM RATINGS

Supply voltage Voltage at any pin Operating temperature Storage temperature Package dissipation 7 Volts GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

DC ELECTRICAL CHARACTERISTICS

 T_{Δ} =0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
V _{IL} V _{IH} V _{OL}	Input low level Input high level Output low level	2.0		0.8	V	I _{oL} = 8.0 mA
V _{OH} I _{IL} I _{IH} I _{CC} R _{IN}	Output high level Input low current Input high current Operating current Internal pull-up resistance	2.4	20 680	-1 1 30	MA mA mA KΩ	I _{OH} = 8.0 mA Except pins 2, 10, 12 V _{IN} =Vcc No load. Pins 10,12

PERIPHERAL CLOCK TABLE CHART FOR ST49C155-23 (MHz)

CLK1	CLK2	CLK3	CLK4	
1.843	16	24	12	

FREQUENCY TRANSITIONS

The ST49C155 is designed to provide smooth, glitch-free frequency transitions on the 1XCLK and 2XCLK clocks when the frequency select pins are changed. These frequency transitions are less than 0.1% frequency change per clock period.

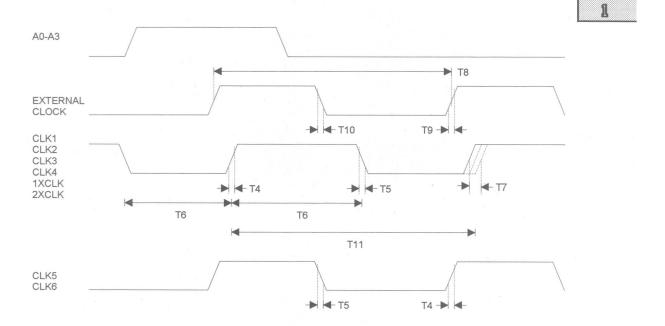
AC ELECTRICAL CHARACTERISTICS

 $T_{A}=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

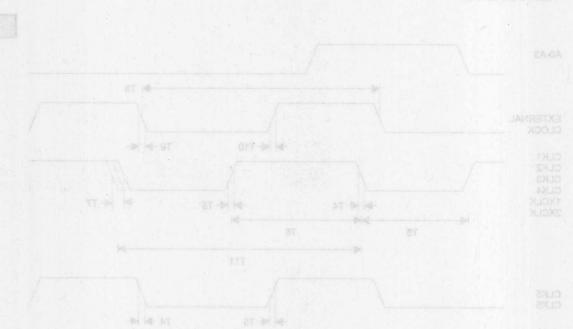
Symbol	Rise time Fall time Duty cycle Duty cycle		Min	Limits Typ	Max	Units	Conditi	ions	
T ₄ T ₅ T ₆ T ₆			40 40	1 1 48/52 48/52	1.5 1.5 60 55	ns ns %	0.8V - 2.0V 2.0V - 0.8V 1.4V switch Vcc/2 switc	point	
T ₇ T ₈ T ₉ T ₁₀	Jitter Input frequer Input clock ri Input clock fr	se time		ni-Wi -	±175 14.318	±300 20 20	ps MHz ns		
10	mput clock is	V		2.0		20		Input Jow let Input high le	
	Am 0.8 = 10 Am 0.8 = 10			24				Output low light	
2, 10,	Except pins	Am		19-54			Inen	Mo wof Jugni	- 4

The ST49C155 is designed to provide smooth, glitch ree frequency transitions on the TXCLK and 2XCLJ clocks when the frequency select pins are changed These frequency transitions are less than 0.1% frequency change per clock period.

TIMING DIAGRAM







Priliminary

ST49C158

Printed September 9, 1994

PREPROGRAMMED CPU MOTHERBOARD FREQUENCY GENERATOR

GENERAL DESCRIPTION

The ST49C158 is a monolithic analog CMOS device designed to generate eight simultaneous clock outputs for mother board and green PC applications. It is designed in a 1.2µ process to achieve 100 MHz operation with low clock jitter. The CPU and 2XCPU outputs are skew controlled within 250 psec.

The ST49C158 is designed for desktop and notebook PC's and supports Energy Star PC's. The ST49C158 can accept 14.318 MHz system clock or external crystal connected between XTAL1 and XTAL2 as the reference clock (reference clock can be changed to generate non-standard frequencies from the standard programmed device).

The ST49C158 is metal mask programmable to provide any custom set of 2XCPU frequencies. The programmed clock outputs are selectable via three address lines for CPU clocks.

SOIC Package

CPU2	1		24	Α0
XTAL2	2	processor and	23	A1
XTAL1	3	er la t	22	CPU1
DVCC	4	4	21	2XCPU
DGND	5	2F2,	20	DVCC
CLK1	6	1580	19	DGND
CLK2	7	9C1	18	BCLK
CPU3	8	ST49C158CF24	17	CPU4
AGND	9	page of the second	16	AVCC
OE	10		15	A2
CPU5	11		14	CPU6
DGND	12	IPA4	13	CPU7

FEATURES

- · Can replace multiple oscillators/crystals
- Pin -to-pin compatible to ICS9158
- · Compatible with 286, 386, and 486 CPUs
- Skew controlled 2X and 1X CPU clocks
- Programmable analog phase locked loop
- High speed (up to 100 MHz output)
- Low power single 5V CMOS technology
- · Smooth and glitch-free clock transitions
- 24 pin PDIP or SOIC package

DIP Package

CPU2	1		24	A0
XTAL2	2		23	A1
XTAL1	3		22	CPU1
DVCC	4	24	21	2XCPU
DGND	5	ST49C158CP24	20	DVCC
CLK1	6	2158	19	DGND
CLK2	7	490	18	BCLK
CPU3	8	S	17	CPU4
AGND	9		16	AVCC
OE	10		15	A2
CPU5	11		14	CPU6
DGND	12		13	CPU7

ORDERING INFORMATION

Part number ST49C158CP24 ST49C158CF24

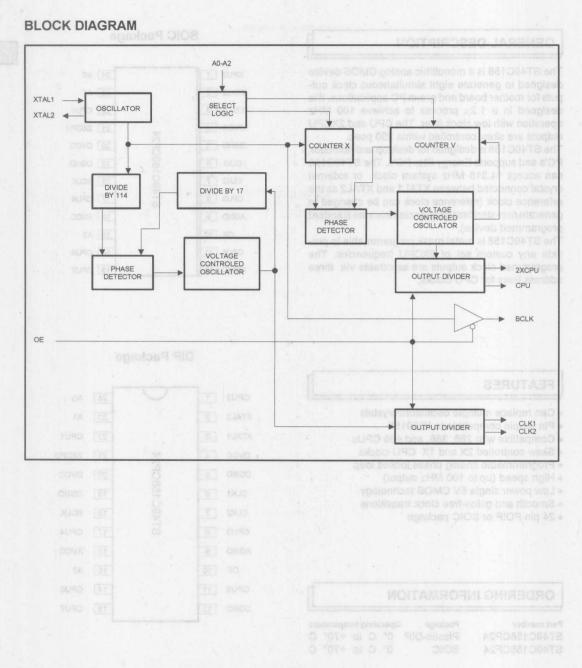
Package

Operating temperature Plastic-DIP 0° C to +70° C

SOIC

0° C to +70° C

STARTECH



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description						
CPU2	1	O Jugluc	CPU clock output.						
XTAL2	2	Output. O	Crystal output.						
XTAL1	cy se S ct ad	SPU globk insquen	Crystal or External clock input.						
DVCC	.0 4 2-nbb	requently select a	Digital supply voltage. Single +5 volts.						
DGND	5	0	Digital signal ground.						
CLK1	6	0	16 MHz clock output.						
CLK2	7	O HERRAL CLO	24 MHz floppy disk clock output.						
CPU3	8	3C158 Oldz)	CPU clock output.						
AGND	9	OLICE CLICE	Analog ground.						
OE	10*	16 24	Output Enable (active high). Low on this pin sets all the outputs to three state mode.						
CPU5	11	QUENO TRANS	CPU clock output.						
DGND		ST490 0 8 sides	Digital signal ground.						
CPU7	g lool13 (on	frequency transitions in the contract of the c							
CPU6	14	e frequency fraits							
A2	15*	1	1X and 2X CPU clock frequency select address 2.						
AVCC	16	1	Analog supply voltage. Single +5 volts.						
CPU4	17	0	CPU clock output.						
BCLK	18	0	Buffered 14.31818 MHz clock output.						
DGND	19	0	Digital signal ground.						
DVCC	20	l i	Digital supply voltage. Single +5 volts.						

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description	
2XCPU	21	Lipqiso	CPU clock output.	2902
CPU1	22	L dia	CPU clock output.	
A1	23*	xternal block input	1X and 2X CPU clock frequency select address 1.	
A0	24*	ly voltatje. Singla	CPU clock frequency select address 0.	

^{*}Have internal pull-up resistor on inputs

ACTUAL OUTPUT FREQUENCIES

CPU CLOCK TABLE FOR ST49C158 (using 14.318 MHz input. All frequencies in MHz).

A2 A1 A0		A0	2XCPU	CPU	
0	0	0	7.58	3.79	
0	0	1	15.51	7.76	
0	1	0	59.87	29.93	
0	1	1	40.09	20.05	
1	0	0	50.11	25.06	
1	0	1	66.47	33.24	
1.	1	0	79.77	39.89	
1	1	1	100.23	50.11	

PERIPHERAL CLOCK TABLE CHART FOR

CLK1	CLK2
16	24

FREQUENCY TRANSITIONS

The ST49C158 is designed to provide smooth, glitchfree frequency transitions on the CPU and 2XCPU clocks when the frequency select pins are changed. These frequency transitions are less than 0.1% frequency change per clock period.

ABSOLUTE MAXIMUM RATINGS

Supply voltage

Voltage at any pin

Operating temperature

Storage temperature

Package dissipation

Supply voltage

GND-0.3 V to VCC+0.3 V

O° C to +70° C

-40° C to +150° C

500 mW

DC ELECTRICAL CHARACTERISTICS

 $T_A = 0^{\circ} - 70^{\circ}$ C, $V_{CC} = 5.0$ V \pm 10% unless otherwise specified.

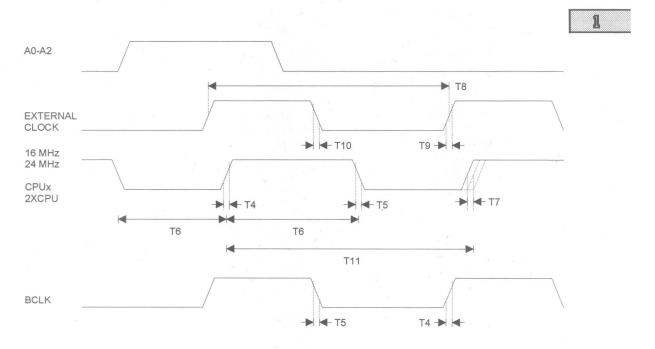
Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
V _{IL} V _{IH} V _{OL} V _{OH}	Input low level Input high level Output low level	2.0	7/F	0.8	mi) pen d mid Vel × V	Los fuerti otà fuerti I _{OL} = 8.0 mA
I _{IL}	Output high level Input low current Input high current Operating current	2.4	70	-40 40	V μA μA mA	I _{OH} = -8.0 mA Except pins 2, 10 V _{IN} = Vcc No load.
R _{IN}	Internal pull-up resistance		680		kΩ	Pin 10

AC ELECTRICAL CHARACTERISTICS

 T_A =0° - 70° C, V_{cc} =5.0 V ± 10% unless otherwise specified.

Symbol	Paramo	eter			Min	Limits Typ	Max	Units	Cond	litions
T ₄ T ₅ T ₆ T ₆	Output rise time Output fall time Duty cycle Duty cycle			bei	40 40	2.5 2.5 48/52 48/52	3 3 60 55	ns ns %	0.8V - 2. 2.0V - 0. 1.4V swit Vcc/2 sw	8V = 00
T ₇ T ₇ T ₈	The second secon			nii	7	±85	±100 500 20	ps ps MHz		
T ₉ T ₁₀	Input clock rise time Input clock fall time			0			20		Input low	V _{IL}
	0.8 = 8.0 0.8 = 8.0 V			è.				w level gh level	Output to Output in	ь. V
	μΑ «Χοερί μα μΑ V = V μΑ No load.	OA-	70					h current	Input high	10 10 11

TIMING DIAGRAM









ST49C214

Printed September 2, 1994

PREPROGRAMMED DUAL VIDEO/MEMORY FREQUENCY GENERATOR

GENERAL DESCRIPTION

The ST49C214 is a monolithic analog CMOS device designed to generate dual frequency outputs from sixteen possible combinations for video Dot clock frequencies and four memory clock frequencies for high performance video display systems. The ST49C214 is a mask option programmable device to provide different output frequencies for custom applications. It is designed with 1.2 process to achieve 130 MHz speed for high end frequencies.

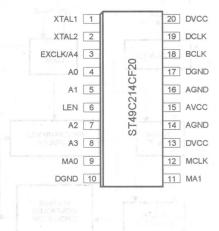
The ST49C214 is designed to replace existing video clocks generated from individual oscillators, to reduce board space and number of oscillators. To provide high speed and low jitter clock, The ST49C214 utilizes high speed analog CMOS phase locked loop using 14.318 MHz system clock as reference clock (reference clock can be changed to generate optional frequencies from standard programmed device) or external crystal connected between XTAL1 and XTAL2.

The ST49C214 can provide optional clock frequencies, utilizing single layer metal mask option. The programmed clock outputs are selectable via four address lines and address latch enable pin for video Dot clock selection and two address lines for memory clock selection.

FEATURES

- Can replace multiple oscillators/crystals
- Pin -to-pin compatible to ICS2494, AV9194
- Programmable analog phase locked loop
- High speed (up to 130 MHz output)
- Low power single 5V CMOS technology
- 20 pin dip or SOIC package

SOIC Package



Plastic-DIP Package

	20 DVCC
1	19 DCLK
0	18 BCLK
,P2(17 DGND
140	16 AGND
9C2	15 AVCC
ST4	14 AGND
, ,	13 DVCC
	12 MCLK
	11 MA1
	ST49C214CP20

ORDERING INFORMATION

 Part number
 Package
 Operating temperature

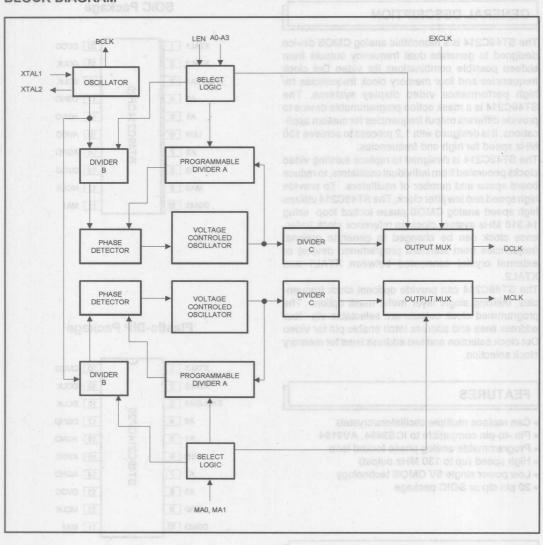
 ST49C214CP20-xx
 Plastic-DIP
 0° C to +70° C

 ST49C214CF20-xx
 SOIC
 0° C to +70° C

 ST49C214CJ20-xx
 PLCC
 0° C to +70° C

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BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
XTAL1	TAL1 1		Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock XTAL2 is left open or used as buffered clock output.
XTAL2	2	0	ent gritations not alumed ad F goneon
EXCLK	3*	1	External clock input. (3.8\A) × photo socores and
A0	4*	1	Dot clock Frequency select address 1.
A1	5*	1	Dot clock Frequency select address 2.
LEN	6*	, 1	Address latch enable input (active high). To latch selected programmed clock output.
A2	7*	1	Dot clock Frequency select address 3.
A3	8*	1	Dot clock Frequency select address 4.
MAO	9*	. 1	Memory clock Frequency select address 1.
GND	10	0	Digital and Analog ground.
MA1	11*	1	Memory clock Frequency select address 2.
MCLK	12	0	Programmed memory clock output frequency.
DVCC	13	1	Digital supply voltage. Single +5 volts.
GND	14	0	Digital and Analog ground.
AVCC	15	1	Analog supply voltage. Single +5 volts.
GND	16	0	Digital and Analog ground.
GND	17	0	Digital and Analog ground.
BCLK	18*	0	Buffered crystal clock output frequency.
DCLK	19	0	Programmed video clock output frequency.
DVCC	20	. 1	Digital supply voltage. Single +5 volts.

^{*} Have internal pull-up resistor on inputs.

FREQUENCY SELECT CALCULATION

The ST49C214 contains an analog phase locked loop circuit with a digital closed loop divider and a final series divider to achieve desired dividing ratios for clock output.

The accuracy of the frequencies produced by the ST49C214 depends on the input frequency and final output frequency. The formula for calculating the exact output frequency is as follows:

XCLK = (Reference clock) X (A/B.C)

where A=1,2,3,......127, B=1,2,3,......127, AND C=1,2,4

For proper output frequency, the ST49C214 can accept reference frequency from 5 - 40 MHz and divider ratio up to 15.

MASK OPTIONS assemble the less vonemper? About vrome M

The following mask option are provided for custom applications.

*Any frequency can be in any decoding position.

ABSOLUTE MAXIMUM RATINGS

Supply range 7 Volts
Voltage at any pin GND-0.3 V to VCC+0.3 V
Operating temperature 0°C to +70°C
Storage temperature -40°C to +150°C
Package dissipation 0°M

DC ELECTRICAL CHARACTERISTICS

 $T_a=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Parameter Limits		May	Units	Conditions		
30 00	#1175 ±3	IVIIII	тур	IVIAX		114 111
Input low level		14.21		0.8	V	13.100
Input high level		2.0			V	wort in E
Output low level				0.4	V	$I_{01} = 8.0 \text{ mA}$
Output high level		2.4			V	$I_{OH} = 8.0 \text{ mA}$
Input low current		-	-	-350	Α	Except crystal
						input
			20000	1		V _{IN} =Vcc
Operating current			20	30	mA	No load.
						DCLK=80MHz,
Internal null up register		4.5	20	25	1/	MCLK=40MHz
	Input low level Input high level Output low level Output high level Input low current Input high current Operating current	Input low level Input high level Output low level Output high level Input low current Input high current	Input low level Input high level Output high level Output high level Input low current Input high current Operating current	Input low level Input high level Output low current Input high current Operating current 20	Input low level Input high level Output high level Output high level Input low current Input high current Operating current Operating current 20 30 Min Typ Max 0.8 0.8 0.8 0.8 0.4 0.4 0.4 0.4 0.4 0.4 0.4 0.4 0.4 0.4	Input low level 0.8 V 10.5 10

1

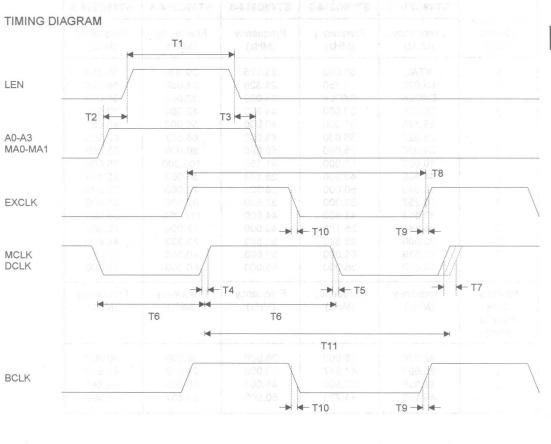
AC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70°C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
Т,	Enable pulse width	20			ns	
T ₂ T ₃ T ₄	Setup time data to enable	20	STICS	CTER	ns	C ELECTRICAL
T ₃	Hold time to data enable	10			ns	
T ₄	Rise time	a specified.	otin bewig	1.5	ns	0.8V - 2.0V
T ₅	Fall time		1	1.5	ns	2.0V - 0.8V
T ₆	Duty cycle	40	48/52	60	%	1.4V switch point
T ₆ notin	Duty cycle	45	48/52	55	%	Vcc/2 switch point
-	yp Max	er gild				
T ₇ T ₈ T ₉	Jitter		±8175	±300	ps	
18	Input frequency	14.318	3	32	MHz	wet tugniV
19	Input clock rise time	2.0		20	ns	agirl tugnir V
T ₁₀ An	Input clock fall time			20	ns	V _a Output low
T ₁₁ AIT	Output frequency change	AS.	0.005	1 500	%	of tugtuo V

Operating current





\ C. d L L.	ST49C214-1	ST49C214-2	ST49C214-3	ST49C214-4	ST49C214-5
Video clock address (Hex)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	XTAL	30.000	25.175	20.000	50.350
1	65.028	77.250	28.325	24.000	56.644
2	EXCLK	EXCLK	85.000	32.000	65.000
3	36.000	80.000	44.900	40.000	72.000
4	25.175	31.500	40.000	50.000	80.000
5	28.322	36.000	48.000	66.667	89.800
6	24.000	75.000	50.000	80.000	63.000
. 7	40.000	50.000	81.150	100.000	75.000
8	44.900	40.000	25.175	54.000	25.175
9	50.350	50.000	28.325	70.000	28.322
Α	16.257	32.000	37.500	90.000	31.500
В	32.514	44.900	44.900	110.000	36.000
C	56.644	25.175	40.000	25.000	40.000
D	20.000	28.322	32.500	33.333	44.900
E	41.539	65.000	50.000	40.000	50.000
F	80.000	36.000	65.000	50.000	65.000
Memory clock address (Hex)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	32.900	36.000	36.000	16.000	40.000
1	35.600	44.347	40.000	24.000	41.612
2	43.900	37.500	45.000	50.000	44.744
3	49.100	44.773	50.000	66.667	50.000
	T9-14-14	F-T10	19-		

Compatible with	ICS-236 AV-36	ICS-242 AV-42	ICS-231	ICS-244 AV-44	ICS-237
Video Controller	GD6410	WD90C30	ET4000		ET4000

25"	ST49C214-6	ST49C214-8	ST49C214-9	ST49C214-10	ST49C214-10
Video clock address (Hex)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)
0	25.175	25.175	25.175	30.250	XTAL
1	28.322	28.322	28.322	65.000	16.257
2	00.40.000	40.000	40.000	85.000	EXCLK
3	65.000	32.500	EXCLK	36.000	32.514
4	44.900	50.000	50.000	009.25.175	000.25.175
5	50.000	65.000	77.000	000 28.322	28.322
6	00130.000	38.000	36.000	34.000	24.000
7	75.000	44.900	44.889	88 40.000	40.000
8	25.175	31.500	00.0130.00	44.900	OCC XTAL
9	28.322	36.000	00.0120.00	50.350	16.257
Α	O EXCLK	000.08	000.08	31.500	EXCLK
В	EXCLK	63.000	31.500	32.500	36.000
С	60.000	50.000	0.0110.00	63.000	25.175
D	000.08	100.000	65.000	72.000	28.322
E	O EXCLK	76.000	75.000	75.000	24.000
F	O EXCLK	00110.000	72.000	000.08 500	40.000
Memory	Frequency	Frequency	Frequency	Frequency	Frequency
clock address (Hex)	(MHz)	as Ha(MHz)	(MHz)	(MHz)	(MHz)
0	000 50.000	70.000	55.000	36.000	31.000
1	60.000	63.830	75.000	000 44.000	36.000
2	65.000	60.000	70.000	49.000	43.000
3	75.000	81.000	80.000	40.000	00 49.000

Compatible with	ICS-253	ICS-263	ICS-256	ICS-266	ICS-247
Compatible with	103-253	103-203	103-256	103-200	103-247
			AV-56		
Video Controller	NCR77C22E	HT216	S3/86C911	GDS5410	GDS5320

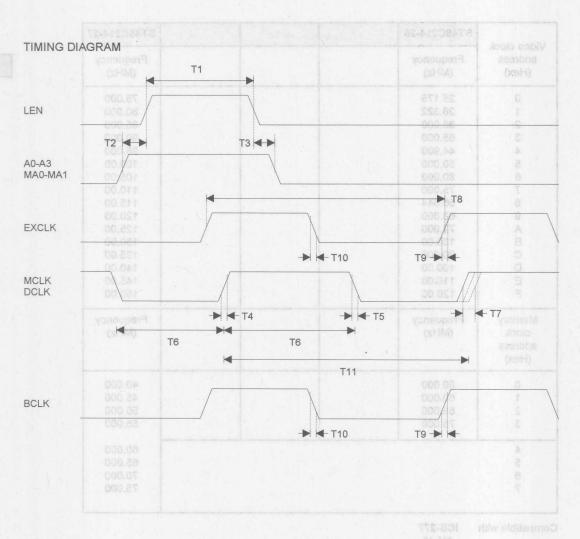
ar	ST49C214-17	ST49C214-18	ST49C214-19	ST49C214-20	ST49C214-25*		
Video clock address (Hex)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Video clo address (Hex)	
0	25.175	25.175	25.175	50.350	25.175	0	
1	28.322	28.322	28.322	56.644	28.322		
2	28.636	40.000	40.000	33.250	40.000	2	
3	36.000	EXCLK	EXCLK	52.000	72.000	3	
4	40.000	50.000	50.000	80.000	50.000	4	
5	42.954	77.000	77.000	63.000	77.000	8	
6	44.900	36.000	36.000	EXCLK	36.000	8	
7	57.272	44.889	44.889	75.000	44.900	7	
8	60.000	130.00	130.00	25.175	130.00	8	
9	63.960	120.00	120.00	28.322	120.00	8	
A	75.000	80.000	80.000	31.500	80.000	A	
В	80.000	31.500	31.500	36.000	31.500	8	
C	85.000	110.00	110.00	40.000	110.00	0	
D	99.000	65.000	65.000	44.900	65.000	0	
E	102.00	75.000	75.000	50.000	75.000	3	
F	108.00	94.500	94.500	65.000	94.500	3	
Memory clock address (Hex)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	Frequency (MHz)	(normalifi clock saidmas (xal-l)	
0	64.000	45.000	55.000	40,000	55,000	0	
U		38.000	75.000	33.333	65.000		
1	40.830	30.000					
	40.830 48.000	52.000	70.000	44.000	70,000	2	

Compatible with	ICS-240	ICS-275 AV-07	ICS-305	ICS-260	CH9294-G
Video Controller	TI/34010/20	S3/801/805	S3/924	WEITEK W5186	\$3/801/805

	ST49C214-26				ST49C214-2
Video clock address (Hex)	Frequency (MHz)				Frequency (MHz)
0	25.175		17		75.000
1	28.322				80.000
2	36.000				85.000
3	65.000		13 N S		90.000
4	44.900				95.000
5	50.000		/		100.00
6	80.000		/ / / /		105.00
7	75.000				110.00
8	56.644		,	Ban	115.00
9	63.000				120.00
Α	72.000		7		125.00
В	130.00			1	130.00
С	90.000		4		135.00
D	100.00				140.00
E	110.00				145.00
F	120.00			1	150.00
Memory	Frequency	at → N		p. 42	Frequency
clock	(MHz)	4			(MHz)
address			87		
(Hex)				\$r	×
0	50.000				40.000
1	60.000		7		45.000
2	65.000				50.000
3	75.000				55.000
4					60.000
5					65.000
6					70.000
7					75.000

Compatible with ICS-277
AV-46
Video Controller NCR77C22E+

^{*=} The External clock input pin has been changed to MA2 to privide four additional preprogrammed memory clock selections. When Pin-3 of the ST49C214-25 is connected to ground it is downward compatible to standard ST49C214-XX. This pin contains internal pull-up resistor.



^{*=}The External clock input pin has been changed to thA2 to privide four additional preprogrammed memory clock selections. When Pin-3 of the ST49C214-25 is connected to ground it is downward compatible to standard ST49C214-XX. This our contains intercel null-up resistor.

PREPROGRAMMED STEREO CODEC's CLOCK SYNTHESIZER

DESCRIPTION

The ST49C418 is a mask programmable monolithic analog CMOS device, designed to replace existing dual crystals/oscillators with single frequency clock input. The ST49C418 provides high speed and low jitter clock outputs for multi-media stereo codecs.

The ST49C418 interfaces to Analog Devices's AD1848 and Crystal Semiconductor's CS4231 stereo codecs. The ST49C418 provides 16.934 and 24.576 MHz clock outputs utilizing the 14.318 MHz clock input.

ST49C418 is designed in a 1.2 μ process to achieve 150 MHz speed for high end frequencies.

SOIC Package

REFCLK 1 8 GND

VCC 2 9 7 VCC

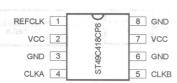
GND 3 6 GND

CLKA 4 5 CLKB

FEATURES

- Programmable analog phase locked loop
- Low power single 5V CMOS technology
- 8 pin DIP or SOIC package
- Programmable input/output frequencies
- TTL compatible outputs
- No external components besides de-coupling capacitors

Dip Package



ORDERING INFORMATION

Part number ST49C418CP8 ST49C418CF8 Package Operating temperature
Plastic-DIP 0 ° C to +70° C
SOIC 0° C to +70° C

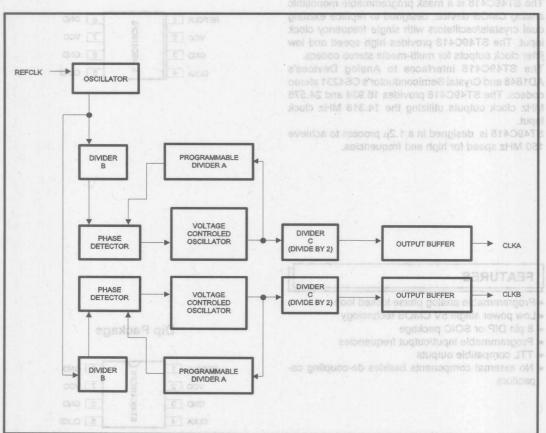
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STARTECH

PREPROGRAMMED STERED CODEC'S CLOCK SYNTHESIZER

BLOCK DIAGRAM

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ORDERING INFORMATION
Part number Package Operating temperature
ST49C418CP8 Plastic-DIP 0 ° C to +70° to 470° t

SYMBOL DESCRIPTION

Symbol	. Pin	Signal Type	Pin Description
REFCLK	1	1	External Reference Clock input. REFCLK is used as internal phase locked loop reference clock.
VCC	2	1	Supply voltage. Single +5 volts.
GND	3	0	Supply ground.
CLKA	4	innits O	Programmable output clock. Programmed for 16.9344 MHz output.
CLKB	5	8.00	Programmable output clock. Programmed for 24.576 MHz output.
GND	6	0	Supply ground.
VCC	porew 7 Au	1 25	Supply voltage. Single +5 volts.
GND	8	0	Supply ground.

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect 0.01 to 0.047 μF capacitor to REFCLK, and keep the lead length of the capacitor to REFCLK to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C418 contains an analog phase locked loop circuit with digital closed loop dividers and a final output divider to achieve the desired dividing ratios for the clock output.

The accuracy of the frequencies produced by the ST49C418 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLOCK = (Reference clock) X A/(B.C)

where A=5, 6, 7,......128 B=5, 6, 7,......128 C=2

For proper output frequency, the ST49C418 can accept a reference frequency from 5 - 40 MHz and divider ratio up to 15.

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
	-40° C to +150° C
Package dissipation	500 mW
131 103330 1	

DC ELECTRICAL CHARACTERISTICS

 T_A =25° C, V_{cc} =5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Condition	ns
V _{IL}	Input low level	2.0		0.8	V		KB
V _{IL} V _{IH} V _{OL} V _{OH}	Output low level	2.8		0.5	V	I _{OL} = 25 mA I _{OH} = 25 mA	
I _{IH}	Input high current Operating current	Supply voltag	20	1 25	μA mA	No load.	

AC ELECTRICAL CHARACTERISTICS

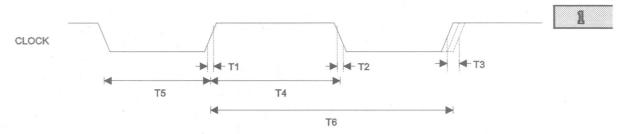
 T_A =25° C, V_{cc} =5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
T ₁ T ₂ T ₄ T ₅ T ₃ T T ₆	CLOCK rise time CLOCK fall time Duty cycle Duty cycle Jitter Input frequency CLOCK frequency change	40 45 5	1 1 48/52 48/52 ±175 10 0.01	1.5 1.5 60 55 ±300 40	ns ns % % ps MHz %	0.5V - 2.8V 2.8V - 0.5V 1.4V switch point VCC/2 switch point

ST49C418

ST49C418

TIMING DIAGRAM



ET PL 14

TIMING DIAGRAM

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LINE DRIVERS / RECEIVERS

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LINE DRIVERS / RECEIVERS

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ST26C31

Printed September 6, 1994

QUAD RS-422 CMOS DIFFERENTIAL LINE DRIVER

DESCRIPTION

The ST26C31 is a CMOS quad differential line driver designed to meet the standard RS-422 requirements and digital data transmission over balanced lines. To improve noise margin and output stability for slow changing input signals special hysteresis is built in the ST26C31 circuit.

The ST26C31 is a high speed CMOS line driver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 digital data transmission applications. ST26C31 is suitable for low power 5V operation with high input voltage protection devices.

SOIC package

INPUT A 1		16 VCC
OUTPUT A+ 2		15 INPUT D
OUTPUT A- 3	CF16	14 OUTPUT D+
ENABLE 4	7	13 OUTPUT D-
OUTPUT B- 5	63	12 ENABLE*
OUTPUT B+ 6	ST26C3	11 OUTPUT C-
INPUT B 7	A Tu	10 OUTPUT C+
GND 8		9 INPUT C

2

FEATURES

- Pin-to-pin compatible with National DS26C31C
- Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422 requirements
- Low propagation delays
- High speed

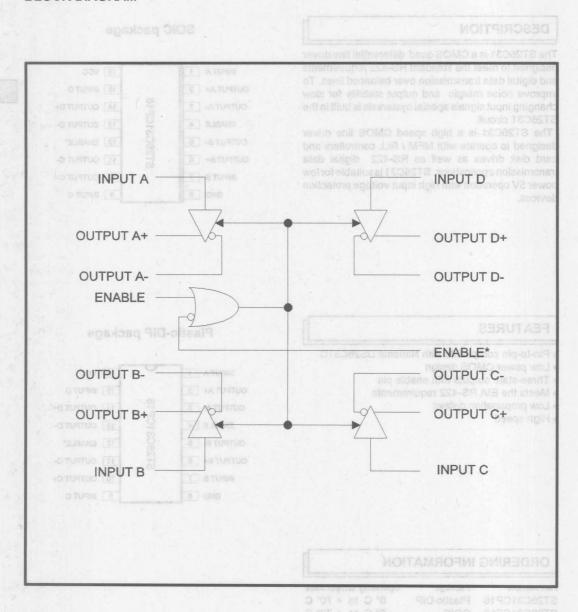
Plastic-DIP package

INPUT A 1	8.7	16 VCC
OUTPUT A+ 2		15 INPUT D
OUTPUT A- 3	P16	14 OUTPUT D+
ENABLE 4	31Cl	13 OUTPUT D-
OUTPUT B- 5	903	12 ENABLE*
OUTPUT B+ 6	ST2	11 OUTPUT C-
INPUT B 7		10 OUTPUT C+
GND 8		9 INPUT C

ORDERING INFORMATION

4		
Part number	Package	Operating temperature
ST26C31CP16	Plastic-DIP	0° C to +70° C
ST26C31CF16	SOIC	0° C to + 70° C
ST26C31IP16	Plastic-DIP	-40° C to +85° C
ST26C31IF16	SOIC	-40° C to +85° C

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT A	1	1	Driver A input pin.
OUTPUT A+	2	0	Driver A differential non-inverting output pin.
OUTPUT A-	3	0	Driver A differential inverting output pin.
ENABLE	4	1	Gate control (active high). This pin is one of the two control pins which enables or disables all four drivers. All four drivers are gated with two input or gate.
OUTPUT B-	5	0	Driver B differential inverting output pin.
OUTPUT B+	6	0	Driver B differential non-inverting output pin.
INPUT B	7	1, 2, 1	Driver B input pin.
GND	8	0	Signal and power ground.
INPUT C	9	1	Driver C input pin.
OUTPUT C+	10	0	Driver C differential non-inverting output pin.
OUTPUT C-	11	0	Driver C differential inverting output pin.
ENABLE*	12	1	Gate control (active low). See ENABLE pin description.
OUTPUT D-	13	0	Driver D differential inverting output pin.
OUTPUT D+	14	0	Driver D differential non-inverting output pin.
INPUT D	15	Top I wax	Driver D input pin.
vcc	16	77 I - 8	Power supply pin.

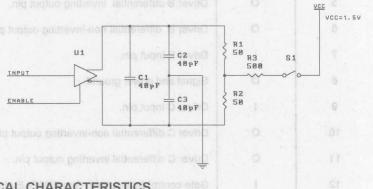
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Functional table

Enable	Enable*	Input	Differential Non-Inverting Output	Differential Inverting Output
	H	X	Z	Z
	L	L	L	H
	L	H	H	mgLugai
	L	L	L	H

X=Don't care synt and lie seldes to seld the northward

Z=Three state (high impedance)



AC ELECTRICAL CHARACTERISTICS

 $T_a=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
T	Propagation delay, input to output	Power	8	10	ns	S1 open
T _o	Differential output rise and fall time		8	10	ns	S1 open
T,	Output enable time		18	20	ns	S1 close
T ₄	Output disable time		18	20	ns	S1 close
*T ₅	Skew		4.2	2	ns	S1 open

^{*} Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

ABSOLUTE MAXIMUM RATINGS

Supply range Voltage at any pin Operating temperature Storage temperature Package dissipation 7 Volts GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

2

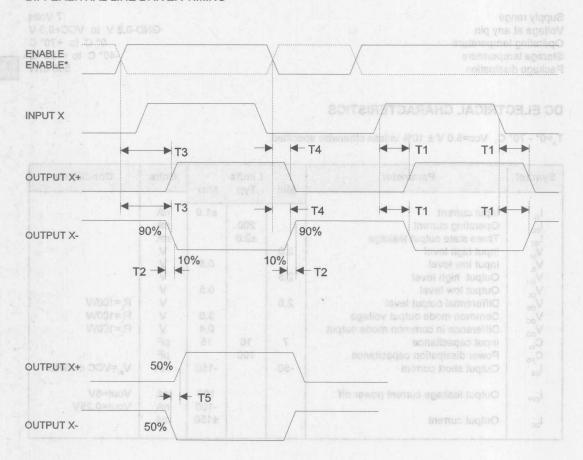
DC ELECTRICAL CHARACTERISTICS

 T_A =0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
I _{IN}	Input current	-Jp e		±1.0	mA	100
Icc	Operating current	S . /	200		mA	
	Three state output leakage		±2.0		mA	Y 11
V _{IH}	Input high level	2.0		-	V	
V.,	Input low level	0,0		0.8	V	
V _{OH}	Output high level	2.5			V	i .
V	Output low level			0.5	V	
Vos	Differential output level	2.0			V	R,=100W
V	Common mode output voltage			3.0	V	R,=100W
V _{od}	Difference in common mode output			0.4	V	R,=100W
CIN	Input capacitance	7	10	15	pF	
C _{PD}	Power dissipation capacitance		100	-	pF	
Ios	Output short current	-30		-150	mA	V _{IN} =VCC or GND
I _{OFF}	Output leakage current power off			100	mA	Vout=6V
				-100	mA	Vout=0.25V
IDC	Output current	3		±150	mA.	

DIFFERENTIAL LINE DRIVER TIMING

ABSOLUTE MAXIMUM RATINGS





ST26C32

Printed September 6, 1994

QUAD RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER

DESCRIPTION

The ST26C32 is a CMOS quad differential line receiver designed to meet the standard RS-422, RS-423 requirements. The ST26C32 has an input sensitivity of 200mv over the common mode input voltage range of $\pm 7V$. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST26C32 circuit.

The ST26C32 is a high speed line receiver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422, and RS-423 differential applications. ST26C32 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments, ST26C32 is suitable for low power 5V operation.

FEATURES

- Pin-to-pin compatible with National DS26C32C
- · Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422 requirements
- Low propagation delays
- High speed

SOIC package

INPUT A- 1		16 VCC
INPUT A+ 2		15 INPUT D-
OUTPUT A 3	CF16	14 INPUT D+
ENABLE 4	32C	13 OUTPUT
OUTPUT B 5	39	12 ENABLE®
INPUT B+ 6	STZ	11 OUTPUT
INPUT B- 7		10 INPUT C+
GND 8		9 INPUT C-

Plastic-DIP package

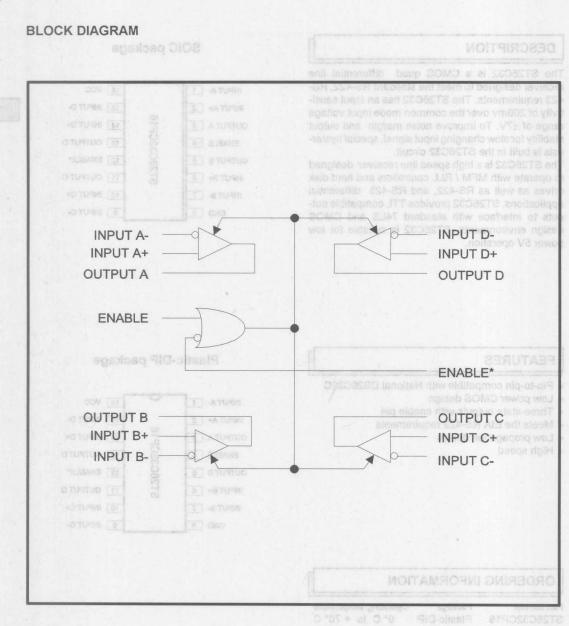
INPUT A- 1		16 VCC
INPUT A+ 2	- F11	15 INPUT D-
OUTPUT A 3	P16	14 INPUT D+
ENABLE 4	35C	13 OUTPUT D
OUTPUT B 5	900	12 ENABLE*
INPUT B+ 6	ST2	11 OUTPUT C
INPUT B- 7		10 INPUT C+
GND 8		9 INPUT C-

ORDERING INFORMATION

Part number	Package	Operating temperature
ST26C32CP16	Plastic-DIP	0° C to + 70° C
ST26C32CF16	SOIC	0° C to + 70° C
ST26C32IP16	Plastic-DIP	-40° C to +85° C
ST26C32IF16	SOIC	-40° C to + 85° C

2

QUAD RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT A-	1	ı	Receiver A differential inverting input pin.
INPUT A+	/ 2	1	Receiver A differential non-inverting input pin.
OUTPUT A	3	0	Receiver A output pin.
ENABLE	4	ı	Gate control (active high). This pin is one of the two control pins which enables or disables all four receivers.
OUTPUT B	5	0	Receiver B output pin.
INPUT B+	6	1 130	Receiver B differential non-inverting input pin.
INPUT B-	7	1 28, 8	Receiver B differential inverting input pin.
GND	8	0	Signal and power ground.
INPUT C-	9	1 10 5	Receiver C differential inverting input pin.
INPUT C+	10	I where	Receiver C differential non-inverting input pin.
OUTPUT C	11	0	Receiver C output pin.
ENABLE *	12	1	Gate control (active low). See ENABLE description
OUTPUT D	13	0	Receiver D output pin.
INPUT D+	14	1	Receiver D differential non-inverting input pin.
INPUT D-	15	1	Receiver D differential inverting input pin.
VCC	16	Linnia Typ Max	Power supply pin.
	ns 31=V ns 31=G ns V _{al} 45	8 10 18 10 19 20 18 20	P rungation dataly, either to output Propagation dataly input to people Out out considerance author disable time

9

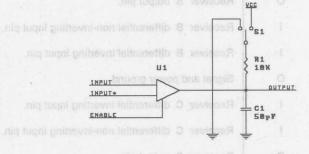
Functional table

2.20				

Enable	Enable*	Output	Differential Non-Inverting Input	Differential Inverting Input
L	Н	Z	X	X
Н	Lo	n hani	entited idverting	HATTEN
Н	L	Н	Н	L
	nia fue	hi paibs	whichon leiter	r A differ

X=Don't care

Z=Three state (high impedance)



AC ELECTRICAL CHARACTERISTICS

 $T_{A}=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min Typ Max		Units	Conditions	
Т,	Propagation delay, input to output		8	10	ns	S1=VCC
T,	Propagation delay, input to putput	4	18	20	ns	S1=GND
T,	Output enable time		18	20	ns	V _{DIF} =2.5V
T ₄	Output disable time		18	20	ns	V _{DIF} =2.5V

ABSOLUTE MAXIMUM RATINGS

Supply range
Voltage at any logic pin
Operating temperature
Storage temperature
Package dissipation

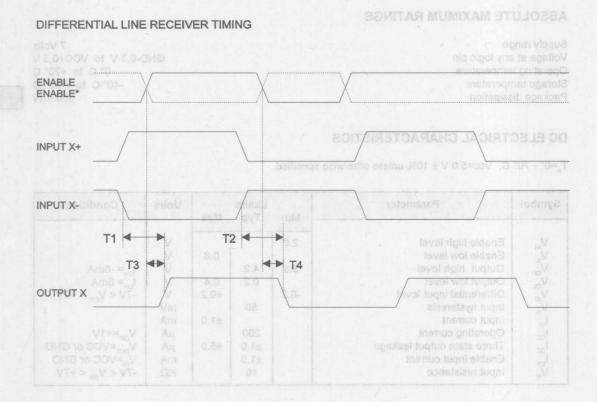
7 Volts GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

2

DC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
V _{IH}	Enable high level	2.0	* 1		V	and the last of
V _{IL}	Enable low level	3.8	> 4.0	0.8	V	1 - 04
V _{OH}	Output high level Output low level	3.0	4.2 0.2	0.4	V	I _{OH} = -6mA I _{OH} = 6mA
V _{ID}	Differential input level	-0.2	0.2	+0.2	V	-7V < V _{CM} < +7V
V _{ID} V _H	Input hysteresis		50		mV	СМ
I _{IN}	Input current			±1.0	mA	
Icc	Operating current		200		μΑ	V _{DIF} =+1V
I_{oz}	Three state output leakage		±1.0	±5.0	μΑ	V _{out} =VCC or GND
I _{EN}	Enable input current		±1.0		mA	V _{IN} =VCC or GND
V _R	Input resistance		10		ΚΩ	$-7V < V_{CM} < +7V$



DUAL RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER AND DRIVER

GENERAL DESCRIPTION

The ST34C50/51 is a CMOS dual differential line receiver and driver, designed to meet the standard RS-422, RS-423 requirements and digital data transmission over balanced lines. The ST34C50/51 has an input sensitivity of 200my over the common mode input voltage range of \pm 7V. To improve noise margin and output stability for slow changing input signal. special hysteresis is built in the ST34C50/51 circuit. The ST34C50/51 is a high speed line receiver and driver, designed to operate with MFM/RLL controllers and hard disk drives as well as RS-422 and RS-423 differential applications, ST34C50/51 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST34C50/51 is suitable for low power 5V operation with minimum board space requirements. ST34C50/51 provides dual differential line receiver with three state control pin and dual line driver with three state control capability.

FEATURES

- Pin -to-pin compatible to Motorola MC34050 and MC34051
- · Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422/423 requirements
- Low propagation delays
- High speed
- Dual line receiver with three state control
- · Dual line driver with three state control

ORDERING INFORMATION

Part number	Package	Operating temperature
ST34C50CP16	Plastic-DIP	0° C to +70° C
ST34C50CF16	SOIC	0° C to +70° C
ST34C50IP16	Plastic-DIP	-40° C to +85° C
ST34C50IF16	SOIC	-40° C to +85° C
ST34C51IP16	Plastic-DIP	-40° C to +85° C
ST34C51IF16	SOIC	-40° C to +85° C

SOIC Package

INPUT A- 1		16 VCC
INPUT A+ 2		15 INPUT D-
OUTPUT A 3	CF16	14 INPUT D+
ENABLE A*/B* 4	50C	13 OUTPUT D
OUTPUT B 5	4C	12 ENABLE C/D
INPUT B+ 6	ST3	11 OUTPUT C
INPUT B- 7		10 INPUT C+
GND 8		9 INPUT C-

ST34C50CF

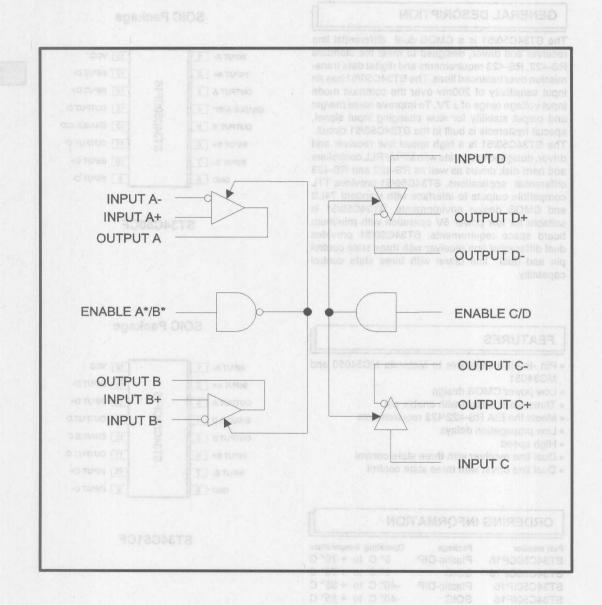
SOIC Package

INPUT A- 1	-	16 VCC
INPUT A+ 2	8 10	15 INPUT D-
OUTPUT A 3	F16	14 INPUT D+
ENABLE D 4	51C	13 OUTPUT
OUTPUT B 5	75 75	12 ENABLE C
INPUT B+ 6	STS	11 OUTPUT
INPUT B- 7		10 INPUT C+
GND 8		9 INPUT C-

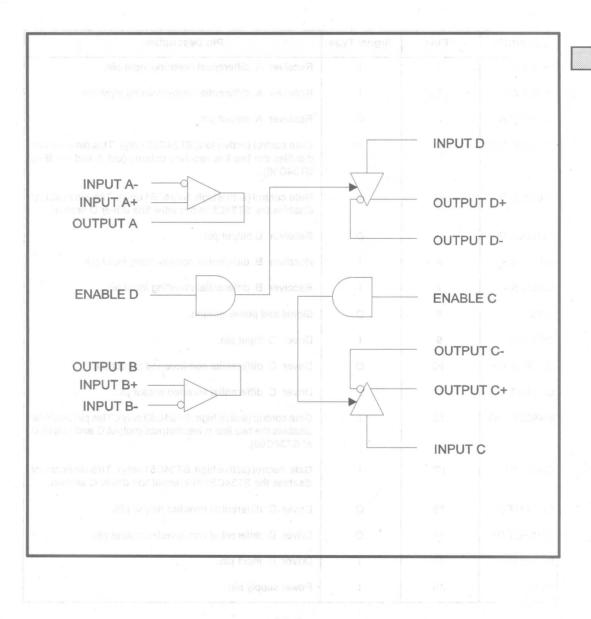
ST34C51CF

9)

ST34C50 BLOCK DIAGRAM



ST34C51 BLOCK DIAGRAM



2

ST34C50 ST34C51

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT A-	1	1	Receiver A differential inverting input pin.
INPUT A+	2	1	Receiver A differential non-inverting input pin.
OUTPUT A	3	0	Receiver A output pin.
ENABLE A/B	1TU9141 =	1	Gate control (active low, ST34C50 only). This pin enables/ disables the two line receiver outputs (out A and out B of ST34C50).
ENABLE D	U97L4*	L.	Gate control (active high, ST34C51 only). This pin enables/ disables the ST34C51differential line driver D section.
OUTPUT B	U9TU5	0	Receiver B output pin.
INPUT B +	6	1	Receiver B differential non-inverting input pin.
INPUT B -	7		Receiver B differential inverting input pin.
GND	8	0	Signal and power ground.
INPUT C	9	1	Driver C input pin.
OUTPUT C+	10	0	Driver C differential non-inverted output pin.
OUTPUT C-	USTUM -	0	Driver C differential inverted output pin.
ENABLE C/D	12		Gate control (active high, ST34C50 only). This pin enables/ disables the two line driver outputs (output C and output D of ST34C50).
ENABLE C	12*	1	Gate control (active high, ST34C51 only). This pin enables/disables the ST34C51differential line driver C section.
OUTPUT D -	13	0	Driver D differential inverted output pin.
OUTPUT D+	14	0	Driver D differential non-inverted output pin.
INPUT D	15	T	Driver D input pin.
VCC	16	1	Power supply pin.

9)

Receiver Functional table (ST34C50 only)

Enable A/B	Output	Differential Non-Inverting Input	Differential Inverting Input
H	Z	X	X X Y
L	L	L	
L	H	H	

X=Don't care

Z=Three state (high impedance)

Receive sections of the ST34C51 are enabled all the time.

Driver Functional table (ST34C50 only)

Enable C/D	Input	Differential Non-Inverted Output	Differential Inverted Output	
L H	X	Z crary disputs	Z Hara (Hara)	delays between

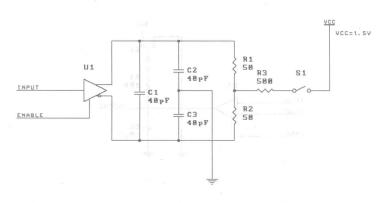
*Driver Functional table (ST34C51 only)

Enable C or D	Input	Differential Non-Inverted Output	Differential Inverted Output
L	X	Z	Z
H	L	L	H
H	H	H	L

X=Don't care

Z=Three state (high impedance)

ST34C50/51 DRIVER AC TEST CIRCUIT



^{*} for each section of ST34C51.

AC ELECTRICAL CHARACTERISTICS

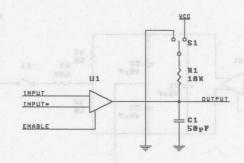
 $T_A=0^{\circ}$ - 70°C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditi	ons
	Line driver section			4	H	H	
Т,	Propagation delay, input to output		8	10	ns	S1 open	
T _o	Differential output rise and fall time		8	10	ns	S1 open	
T,	Output enable time		18	20	ns	S1 close	
T,	Output disable time	emit out I	18	20	ns	S1 close	
T ₂ T ₃ T ₄ *T ₅	Skew			2	ns	S1 open	
	Line receiver section						
	*Driver Functional table (ST34C5		(yli	io 0000	able (ST3	Functional t	
Τ,	Propagation delay, input to output		8	10	ns	S1=VCC	
T, use	Propagation delay, input to putput		18	20	ns	S1=GND	
T ₃	Output enable time		18	20	ns	V _{DIF} =2.5V	
TANDING	Output disable time		18	20	ns	V _{DIF} =2.5V	

^{*} Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

ST34C50/51 RECEIVER AC TEST CIRCUIT

Z=Three state (nigh impedance)



ABSOLUTE MAXIMUM RATINGS

Operating supply range Voltage at any pin Operating temperature Storage temperature Package dissipation 7 Volts GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

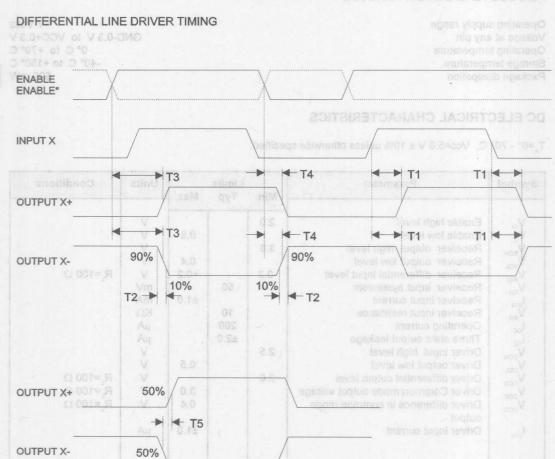
2

DC ELECTRICAL CHARACTERISTICS

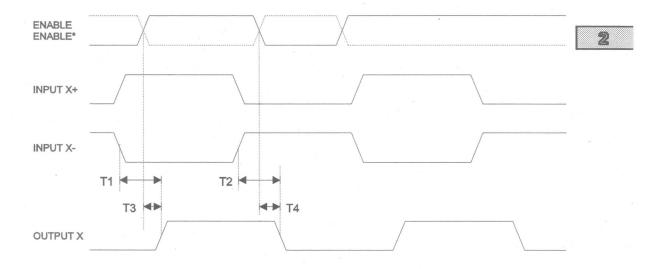
 $T_a=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
VIH VIL VROH VROL VRID VRH IRIN VRR ICC IOZ VDOH VDOS VDOC VDOD	Enable high level Enable low level Receiver output high level Receiver output low level Receiver differential input level Receiver input hysteresis Receiver input current Receiver input resistance Operating current Three state output leakage Driver input high level Driver output low level Driver differential output level Driver Common mode output voltage Driver difference in common mode	2.0 3.8 -0.2 2.5 2.0	50 10 200 ±2.0	0.8 0.4 +0.2 ±1.0 0.5 3.0 0.4	V V V W MA KΩ μA μA V V	R_L =100 Ω R_L =100 Ω R_L =100 Ω R_L =100 Ω
I _{DIN}	output Driver input current			±1.0	μА	

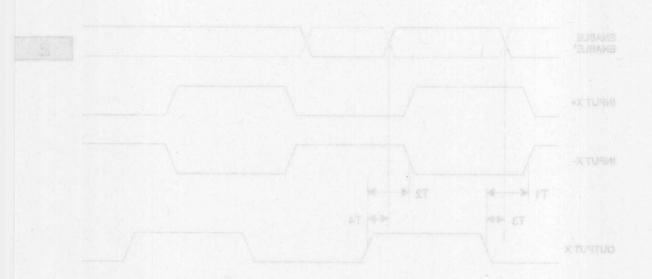
ABSOLUTE MAXIMUM RATINGS



DIFFERENTIAL LINE RECEIVER TIMING



DISFERENTIAL LINE RECEIVER TIMING





ST34C86

Printed September 6, 1994

QUAD RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVER

GENERAL DESCRIPTION

The ST34C86 is a CMOS quad differential line receiver designed to meet the standard RS-422, RS-423 requirements. The ST34C86 has an input sensitivity of 200mv over the common mode input voltage range of \pm 7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST34C86 circuit.

The ST34C86 is a high speed line receiver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 and RS-423 differential applications. ST34C86 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST34C86 is suitable for low power 5V operation.

SOIC package

		_
INPUT A- 1		16 VCC
INPUT A+ 2		15 INPUT D-
OUTPUT A 3	F16	14 INPUT D+
ENABLE A/B 4	386CF1	13 OUTPUT D
OUTPUT B 5	24	12 ENABLE C/I
INPUT B+ 6	STS	11 OUTPUT C
INPUT B- 7		10 INPUT C+
GND 8		9 INPUT C-

FEATURES

- Pin-to-pin compatible with National DS34C86
- Low power CMOS design
- Three-state outputs with enable pin
- · Meets the EIA RS-422 requirements
- Low propagation delays
- High speed TUPINI

Plastic-DIP package

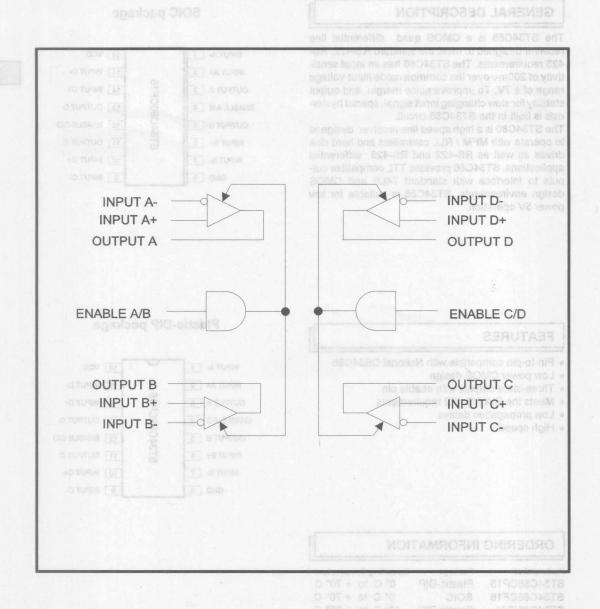
INPUT A- 1	0	16 VCC
INPUT A+ 2	1 8 Tul-	15 INPUT D-
OUTPUT A 3	P16	14 INPUT D+
ENABLE A/B 4	286C	13 OUTPUT D
OUTPUT B 5	27	12 ENABLE C/D
INPUT B+ 6	ST3	11 OUTPUT C
INPUT B- 7		10 INPUT C+
GND 8		9 INPUT C-

ORDERING INFORMATION

Part number	Package	Operating te	mperature
ST34C86CP16	Plastic-DIP	0°C to	+ 70° C
ST34C86CF16	SOIC	0°C to	+ 70° C
ST34C86IP16	Plastic-DIP	-40° C to	+ 85° C
ST34C86IF16	SOIC	-40° C to	+ 85° C

2

BLOCK DIAGRAM



SYMBOL DESCRIPTION

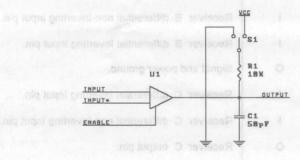
Symbol	Pin	Signal Type	Pin Description
INPUT A-	1	I	Receiver A differential inverting input pin.
INPUT A+	2	1	Receiver A differential non-inverting input pin.
OUTPUT A	3	0	Receiver A output pin.
ENABLE A/B	4	1, 1	Gate control (active high). This pin enables/disables the two line receiver outputs (out A and out B).
оитрит в	5	0	Receiver B output pin.
INPUT B+	6 .	I \ 8	Receiver B differential non-inverting input pin.
INPUT B-	7	1	Receiver B differential inverting input pin.
GND	8	O 18	Signal and power ground.
INPUT C-	9	1.6	Receiver C differential inverting input pin.
INPUT C+	10	I v _{qR3}	Receiver C differential non-inverting input pin.
OUTPUT C	11	0 1	Receiver C output pin.
ENABLE C/D	12	1	Gate control (active high). This pin enables/disables the two line receiver outputs (output C and output D).
OUTPUT D	13	0	Receiver D output pin.
INPUT D+	14	1	Receiver D differential non-inverting input pin.
INPUT D-	15	I	Receiver D differential inverting input pin.
vcc	16	I storie	Power supply pin.

Functional table

Enable A/B C/D	Output	Differential Non-Inverting Input	Differential Inverting Input
L	Z	n Descriptio	X
Н	do Lan	omine Line faith	A Hitero
Н	Н	Н	L

X=Don't care

Z=Three state (high impedance)



AC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
T,	Propagation delay, input to output		8	10	ns	S1=VCC
T,	Propagation delay, input to putput		18	20	ns	S1=GND
T ₃	Output enable time		18	20	ns	V _{DIF} =2.5V
T,	Output disable time		18	20	ns	V _{DIF} =2.5V

ABSOLUTE MAXIMUM RATINGS

Supply range
Voltage at any logic pin
Operating temperature
Storage temperature
Package dissipation

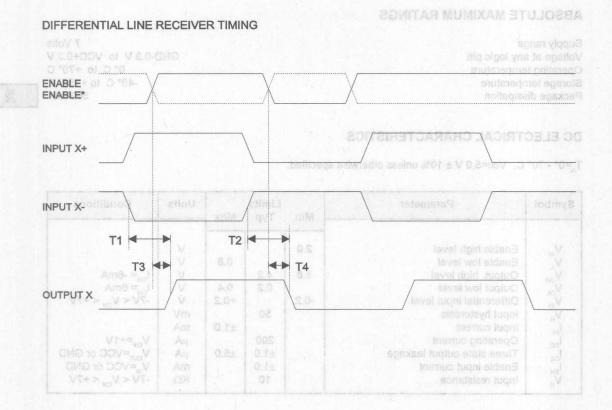
7 Volts GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

7

DC ELECTRICAL CHARACTERISTICS

 $T_*=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
VIH VIL VOH VOL VID VH IN ICC IOZ IEN VR	Enable high level Enable low level Output high level Output low level Differential input level Input hysteresis Input current Operating current Three state output leakage Enable input current Input resistance	2.0 3.8 -0.2	4.2 0.2 50 200 ±1.0 ±1.0 10	0.8 0.4 +0.2 ±1.0 ±5.0	> > > > > m M M M M M M M M M M M M M M	$I_{OH} = -6\text{mA}$ $I_{OH} = 6\text{mA}$ $-7\text{V} < \text{V}_{CM} < +7\text{V}$ $V_{DIF} = +1\text{V}$ $V_{OUT} = \text{VCC or GND}$ $V_{IN} = \text{VCC or GND}$ $-7\text{V} < \text{V}_{CM} < +7\text{V}$





ST34C87

Printed September 12, 19

QUAD RS-422 CMOS DIFFERENTIAL LINE DRIVER

GENERAL DESCRIPTION

The ST34C87 is a CMOS quad differential line driver designed to meet the standard RS-422 requirements and digital data transmission over balanced lines. To improve noise margin and output stability for slow changing input signals special hysteresis is built in the ST34C87 circuit.

The ST34C87 is a high speed CMOS line driver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 digital data transmission applications. ST34C87 is suitable for low power 5V operation with high input voltage protection devices.

SOIC package

INPUT A 1	P.21 St. 2-17 St. 1988 - 1980	16 VCC
OUTPUT A+ 2		15 INPUT D
OUTPUT A- 3	F16	14 OUTPUT D+
ENABLE A/B 4	287CF16	13 OUTPUT D-
OUTPUT B- 5	1 25	12 ENABLE C/D
OUTPUT B+ 6	ST3	11 OUTPUT C-
INPUT B 7	Δ 7	10 OUTPUT C+
GND 8	1 ' ' '	9 INPUT C

- Pin-to-pin compatible with National DS34C87
- Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422 requirements
- Low propagation delays
- High speed

Plastic-DIP package

INPUT A 1	0 -0	16 VCC
OUTPUT A+ 2		15 INPUT D
OUTPUT A- 3	CP16	14 OUTPUT D+
ENABLE A/B 4	37C	13 OUTPUT D-
OUTPUT B- 5	4C8	12 ENABLE C/D
OUTPUT B+ 6	ST3	11 OUTPUT C-
INPUT B 7		10 OUTPUT C+
CND		0 INDUTO

ORDERING INFORMATION

 Part number
 Package
 Operating
 temperature

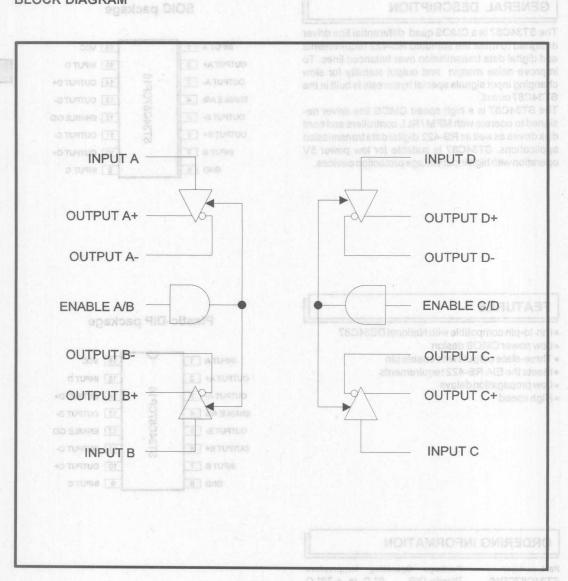
 ST34C87CP16
 Plastic-DIP
 0° C to + 70° C

 ST34C87CF16
 SOIC
 0° C to + 70° C

 ST34C87IP16
 Plastic-DIP
 -40° C to + 85° C

 ST34C87IF16
 SOIC
 -40° C to + 85° C

BLOCK DIAGRAM



9)

SYMBOL DESCRIPTION

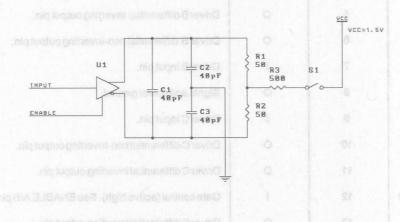
Symbol	Pin	Signal Type	PinDescription
INPUTA	1	1	Driver Ainput pin.
OUTPUTA+	2	0	Driver A differential non-inverting output pin.
OUTPUTA-	3	0	Driver A differential inverting output pin.
ENABLE A/B	4	, 1	Gate control (active high). This pin is one of the two control pins which enables or disables two/four drivers.
ОИТРИТВ-	5	0	Driver B differential inverting output pin.
оитритв+	6	0	Driver B differential non-inverting output pin.
INPUTB	7	Edlard 5	Driver B input pin.
GND	8	0	Signal and power ground.
INPUTC	9	ı	Driver C input pin.
OUTPUTC+	10	0	Driver C differential non-inverting output pin.
OUTPUTC-	11	0	Driver C differential inverting output pin.
ENABLE C/D	12	1 -	Gate control (active high). See ENABLE A/B pin description.
OUTPUTD-	13	0	Driver D differential inverting output pin.
OUTPUTD+	14	0	Driver D differential non-inverting output pin.
INPUTD	15	1	Driver D input pin.
VCC ZnotilendO	16	Jenius Typ Max	Power supply pin.

Functional table

Enable A/B C/D	Input	Differential Non-Inverting Output	Differential Inverting Output
L	X	Z	Z
Н	L	L	n Hoon
Н	Н	Н	L

X=Don't care

Z=Three state (high impedance)



AC ELECTRICAL CHARACTERISTICS

 $T_A = 0^{\circ} - 70^{\circ}$ C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min Typ Max		Units	Conditions	
T,	Propagation delay, input to output		8	10	ns	S1 open
T ₂	Differential output rise and fall time		8	10	ns	S1 open
T ₃	Output enable time		18	20	ns	S1 close
T	Output disable time		18	20	ns	S1 close
*T ₅	Skew			2	ns	S1 open

^{*} Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

ABSOLUTE MAXIMUM RATINGS

Supply range Voltage at any pin Operating temperature Storage temperature Package dissipation 7 Volts GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

<u>l</u>

2

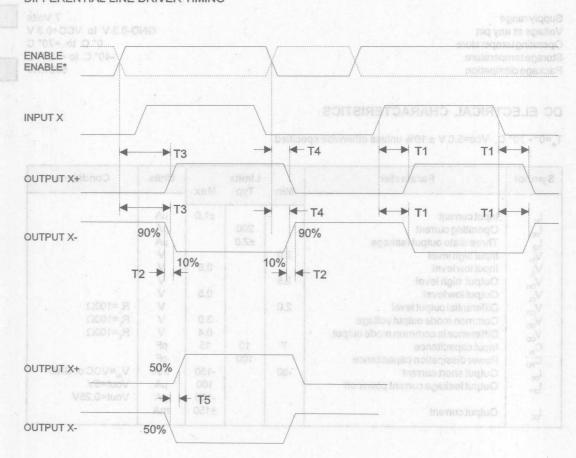
DC ELECTRICAL CHARACTERISTICS

 $T_A = 0^{\circ} - 70^{\circ}$ C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
I _{IN}	Input current	T - Jon to		±1.0	μА	2 2 2
l _{cc}	Operating current	0.0	200		μА	
l ₀₇	Three state output leakage	1.64.5	±2.0		μА	a 10.0 H/
I _{oz} V _{IH}	Input high level	2.0			V	
VIL	InputIowlevel	- OL 20		0.8	V	
V _{OH}	Output high level	2.5			V	
V _{OL}	Output low level			0.5	V	9
Vos	Differential output level	2.0			V	R ₁ =100Ω
V _∞	Common mode output voltage			3.0	V	R =100Ω
V _{op}	Difference in common mode output			0.4	V	R =100Ω
CIN	Input capacitance	7	10	15	pF	
C _{PD}	Power dissipation capacitance		100		pF	
Ios	Output short current	-30		-150	mA	V _{IN} =VCC or GND
l _{off}	Output leakage current power off			100	μА	Vout=6V
G r				-100	μА	Vout=0.25V
I _{DC}	Output current			±150	mA	

DIFFERENTIAL LINE DRIVER TIMING

ABSOLUTE MAXIMUM RATINGS



RS-422, RS-423 CMOS DIFFERENTIAL LINE RECEIVERS AND DRIVERS

GENERAL DESCRIPTION

The ST31C32 is a high speed CMOS combo differential line receiver and driver designed to meet the standard RS-422, RS-423 requirements for digital and transmission over balanced lines. It provides five differential line receivers with three state control and three line drivers also with three state control.

The line driver inputs and line receiver outputs are TTL compatible to interface with standard 74LS and CMOS environments. The ST31C32 has been designed for low power 5 volts operation and is especially suited for MODEM/UART applications.

The receiver in the ST31C32 has an input sensitivity of 200mv over the common mode input voltage range of \pm 7V. They incorporate hysteresis for improved noise margin with slow changing input signals. Input fail-safe circuitry is also included which will cause the output of the receiver to go to a logic "1" level if the inputs are left open.

A special voltage sensing circuit is utilized in the drivers that will three-state the outputs during power down and power up. This will prevent spurious glitches from appearing on the outputs.

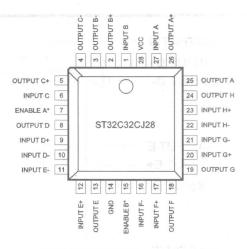
FEATURES

- · Low power CMOS design
- Three-state outputs with enable pin
- Meets the EIA RS-422/423 requirements
- Low propagation delays
- High speed
- Five line receivers with three state control
- Three line drivers with three state control
- 28 pin PLCC and SOIC package

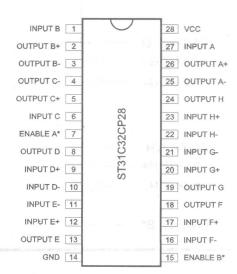
ORDERING INFORMATION

Part number	Package	Operating temperature
ST31C32CJ28	PLCC	0° C to + 70° C
ST31C32CF28	SOIC	0° C to + 70° C
ST31C32IJ28	PLCC	-40° C to +85° C
ST31C32IF28	SOIC	-40° C to +85° C

PLCC Package

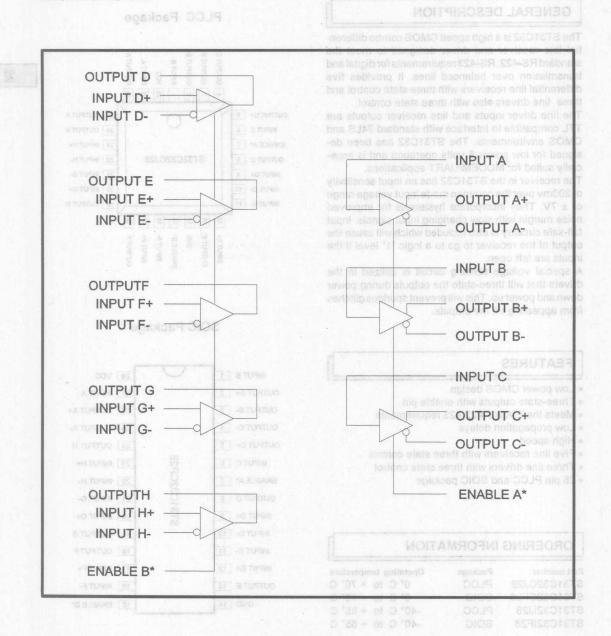


SOIC Package



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BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT B	nverte r input o	r G diferential	Line driver B input pin.
OUTPUT B+	q шслі 2 элэчн	r H di o rential	Line driver B differential non-inverted output pin.
OUTPUT B -	qni beni g /ni-nor	teimenoib H 1	Line driver B differential inverted output pin.
OUTPUT C -	4	nig tu o uo H	Line driver C differential inverted output pin.
OUTPUT C+	niq suqti 5) bəhə	A diffeonial in	Line driver C differential non-inverted output pin.
INPUT C	rgtuo ocenevni-c	A differential no	Line driver C input pin.
ENABLE A*	7*	A inputpur V orc	Gate control A (active low). This pin enables/ disables the three line driver outputs.
OUTPUT D	8	0	Line receiver D output pin.
INPUT D +	9	1	Line receiver D differential non-inverted input pin.
INPUT D -	10	1	Line receiver D differential inverted input pin.
INPUT E -	11	1	Line receiver E differential inverted input pin.
INPUT E +	NO TEST OA 8	1032 RECEIVE	Line receiver E differential non-inverted input pin.
OUTPUT E	13	0	Line receiver E output pin.
GND	14	0	Signal and power ground.
ENABLE B*	15*	1	Gate control B (active low). This pin enables/ disables the five line receiver outputs.
INPUT F -	16	20-1	Line receiver F differential inverted input pin.
INPUT F +	17		Line receiver F differential non-inverted input pin.
OUTPUT F	18	0	Line receiver F output pin.
OUTPUT G	19	0	Line receiver G output pin.
INPUT G +	20	i	Line receiver G differential non-inverted input pin.

9)

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INPUT G -	21	Languaghi 8	Line receiver G differential inverted input pin.
INPUT H - nig h	140 22 vole	ipo tsitos entist od	Line receiver H differential inverted input pin. +8 TUSTIC
INPUT H +	23	e differential love	Line receiver H differential non-inverted input pin.
оитрит н	q juqi24 paha	ni isin Omb s	Line receiver H output pin.
OUTPUT A	25 VIII-	on faith Oattle o	Line driver A differential inverted output pin.
OUTPUT A+	26	.ncopin.	Line driver A differential non-inverted output pin.
INPUT A	elden 27 ig ain	(wolle hos) A	Line driver A input pin.
vcc	28	iver outputs.	Power supply pin.
		nio tuntuo C n	OUTPUT D 8 OTUSTUC

^{*}Has internal pull-up resistor on input

Receiver Functional table and legislation of revision and

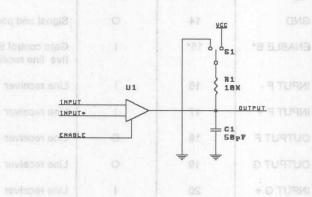
Enable B	Differential Non-Inverting Input	Differential Inverting Input	Output
Н	X	X	Z
L	L	Н	L
L	Н	L	boa Han se

Driver Functional table

Enable A	Input	Differential Non-Inverted Output	Differential Inverted Output
H L L	X L H	Z L H	nig Z glue H

X=Don't care Z=Three state (high impedance)

ST31C32 RECEIVER AC TEST CIRCUIT



AC ELECTRICAL CHARACTERISTICS

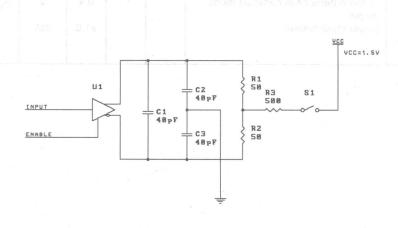
VULTERNY OF VIOLENIE

 $T_A = 0^{\circ} - 70^{\circ}$ C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
T ₁ T ₂ T ₃ T ₄	Line Receiver Timing Propagation delay, input to output Propagation delay, input to putput Output enable time Output disable time	balliooga	8 18 18 18	10 20 20 20	ns ns ns ns	S1=VCC S1=GND V _{DIF} =2.5V V _{DIF} =2.5V
T ₁ T ₂ T ₃ T ₄ T ₅	Line Driver Timing Propagation delay, input to output Differential output rise and fall time Output enable time Output disable time Skew	NIAN -	8 8 18 18 0.5	10 10 20 20	ns ns ns ns ns	S1 open S1 open S1 close S1 close S1 open

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ST31C32 DRIVER AC TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Supply range
Voltage at any pin
Operating temperature
Storage temperature
Package dissipation

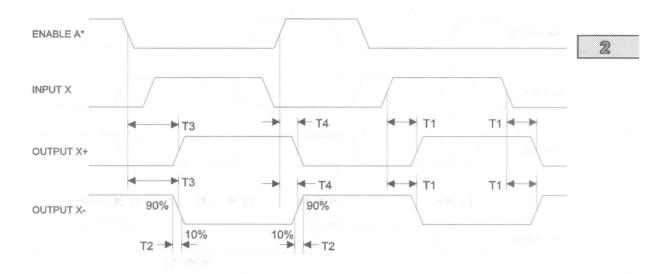
GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

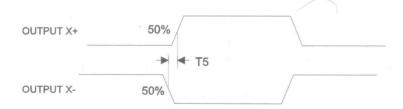
DC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70°C, Vcc=5.0 V ± 10% unless otherwise specified.

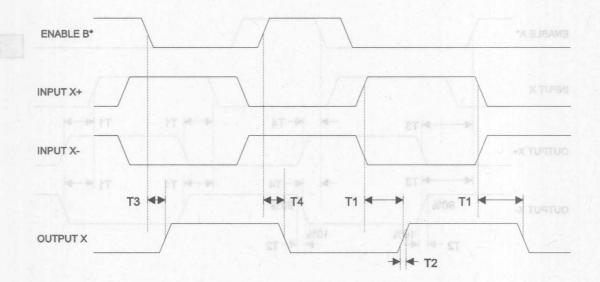
Symbol	Parameter	Min	Limits Typ	Max	Units	Conditio	ns
V _{IH}	Enable high level	2.0			emyside	Output ent	
V _{II}	Enable low level			0.8	em Valde	Output dis	
V _{ROH}	Receiver output high level	3.8			V	Skew	
VPOL	Receiver output low level			0.4	V		
VRID	Receiver differential input level	-0.2		+0.2	V	R _L =100 Ω	
V _{RH}	Receiver input hysteresis		50		mV		
RIN	Receiver input current			±1.0	mA	Carlo Carlo	
V _{RR}	Receiver input resistance		10		ΚΩ	Harris and District	
Icc	Operating current		200		μА		
V _{DOH}	Three state output leakage		±2.0		μА		
V _{DOH}	Driver input high level	2.5		1.3	V		
V _{DOL}	Driver output low level			0.5	V		
V _{DOS}	Driver differential output level	2.0	ात्रव इहर	PETS	V	$R_L=100 \Omega$	
V _{DOC}	Driver Common mode output voltage			3.0	V	R _L =100 Ω	
V _{DOD}	Driver difference in common mode output			0.4	V	$R_L=100 \Omega$	
I _{DIN}	Driver input current			±1.0	mA		
	va ,1=250		e Par V		Was to be		

DIFFERENTIAL LINE DRIVER TIMING





DIFFERENTIAL LINE RECEIVER TIMING



ST -PH M4 -- TS



UARTS 3

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DESCRIPTION

The ST16C450 is a universal asynchronous receiver and transmitter. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C450 is an improved version of the NS16C450 UART with higher operating speed and lower access time. The ST16C450 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C450 provides internal loop-back capability for on board diagnostic testing.

The ST16C450 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

FEATURES

- Pin to pin and functional compatible to NS16450,VL16C450,WD16C450
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- · Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

ORDERING INFORMATION

 Part number
 Package
 Operating temperature

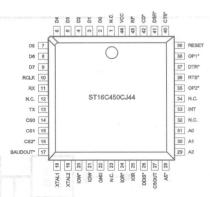
 ST16C450CP40
 Plastic-DIP
 0° C to + 70° C

 ST16C450CJ44
 PLCC
 0° C to + 70° C

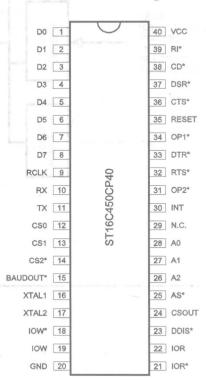
 ST16C450CQ48
 TQFP
 0° C to + 70° C

* Industrial operating range are available.

PLCC Package

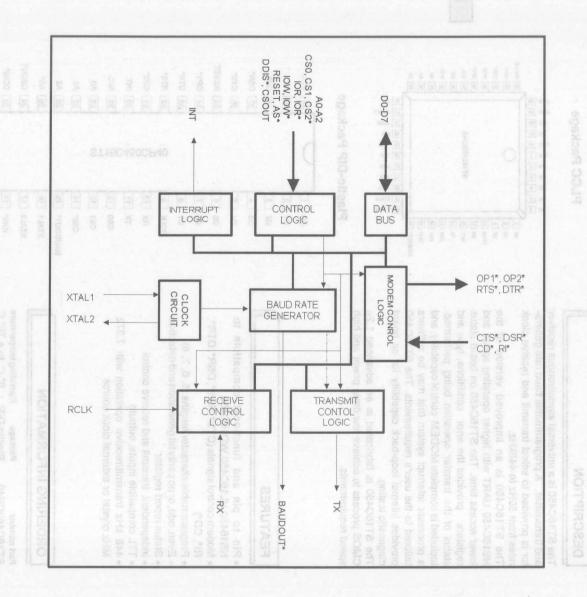


Plastic-DIP Package



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BLOCK DIAGRAM



3-4

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7 ATX 86	1-8 _{0.00} h	ers ta I/O , sug	Bi-directional data bus, Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to
	unto untrol au		be received or transmitted.
RCLK	- GV45 00		Receive clock input. The external clock input to the ST16C450 receiver section if receiver data rate is different from transmitter data rate.
	10	L power ground.	Serial data input. The serial information (data) received from serial port to ST16C450 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX syntax seed fud or group PCI no control (2000)	of and more field 11 (1404 se emas 1707 centra, re (2100/110 min		Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS0	12	I	Chip select 1 (active high). A high at this pin enables the ST16C450 / CPU data transfer operation.
CS1	vor sem igen i each of 13 to sem	ble (active low). Sata Indin II.v St ir et logier	Chip select 2 (active high). A high at this pin enables the ST16C450 / CPU data transfer operation.
the leg	on ac14 or no	has been enac	Chip select 3 (active low). A low at this pin (while CS0=1 and CS1=1) will enable the ST16C450 / CPU data transfer operation.
BAUDOUT*	of the second of	r stoele Oalda er nodw best si.	Baud rate generator clock output. This output provides the 16x clock of the internal selected baud rate. RCLK pin is connected externally to BAUDOUT* pin to provide the receiver clock.
e reusig	n pare 16 mets. Si Isane e toe o n Isane tradicio	loT and Sola	connected to this pin and XTAL2 pin to utilize the internal



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
		nal del¶ bus. Egl	Crystal input 2 or buffered clock output. See XTAL1.
IOW*			Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
rale is different data) received	(receiver data	piock apput. The Preceiver section i mitter data rate. a Input. The seria	Write strobe (active high). Same as IOW*, but uses active high input. Note that only an active IOW* or IOW input is required to transfer data from CPU to ST16C450 during write operation. All the unused pin should be tied to VCC or GND.
GND	20	por to ST16C+5k gic one ond a solic sack mode the RX	Signal and power ground.
IOR*//smeat	21	n and cynnected to boulout. The senal	Read strobe (active low). A low level on this pin transfers the contents of the ST16C450 data bus to the CPU.
IOR ed liw /Cr on a second viscon vis	ool isool deed bel	onal staft, stop and igh) state during in bratsmitter is displ	Read strobe (active high). Same as IOR*, but uses active high input. Note that only an active IOR* or IOR input is required to transfer data from ST16C450 to CPU during read operation. All the unused pin should be tied to VCC or GND.
DDIS*	23 aidt fa dpid A	0	Drive disable (active low). This pin goes low when the CPU is reading data from the ST16C450 to disable the external transceiver or logic's.
CSOUT	iq airti 24 /01/ IO (03/-03)TI	t 3 (a o ve low) A 1) will enable the	Chip select out. A high on this pin indicates that the ST16C450 has been enabled by the chip select pin.
		generator clock ou of the internal sel externally to BA lock.	Address strobe (active low). A low on this pin will latch the state of the chip selects and addressed register (A2-A0). This input is used when signals are not stable for the duration of a read or write operation. If not required, tie the AS* input permanently low.
A2		out 1 or externs of	Address select line 2. To select internal registers.
A1 lo of boso o	27	circuit. An externa	Address select line 1. To select internal registers.
A0	28	cuit end baud rafe;	Address select line 0. To select internal registers.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
N/C	29	rest stand lost	No connection.
INT	30		Interrupt output (active high). This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
OP2*	31	O m ylge	General purpose output (active low). User defined output. See bit-3 modern control register (MCR bit-3).
RTS*	32	0	Request to send (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	33	0	Data terminal ready (active low). To indicate that ST16C450 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
OP1*	34	0	General purpose output (active low). User defined output. See bit-2 of modern control register (MCR bit-2).
RESET	35	Cost El Inge	Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	36 - 1238 - 138 fort	Line Count Modern Los	Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR*	37	Perdaman USB of District	Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.

SYMBOL DESCRIPTION

Symbol Pin		Signal Type	Pin Description				
CD*	38	ction. I	Carrier detect (active low). A low on this pin indicates the carrier has been detected by the modem.				
RI* a naveneriu	nable (Egister) available, trans	y the interrupt e	Ring detect indicator (active low). A low on this pin indicates the modern has received a ringing signal from telephone				
defined or 22V	cuve (04). User	urposeleutput (a	Power supply input.				

All unused input pins should be tied to VCC or GND.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	and the state of the bank	Interrupt Enable Register
0	or to broke	0	Interrupt Status Register	1 90
0	et noto a	1	control function input whose	Line Control Register
1	0	0	STO A TIG STOLE OF THE PARTY	Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	ton 1	Scratchpad Register	Scratchpad Register
0	0	0	MODEM is ready to exchang	LSB of Divisor Latch
0	0		dees not have any effect on t	MSB of Divisor Latch

ST16C450 ACCESSIBLE REGISTERS

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1 921)	IER	0	O TSU)ład Ośsta	0	0 and a per supply of the per	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0	1	0	ISR	nim o s nel an i a di ayon	coro llor en l'acte (SIP) prov	o o file dat ter ter	for o local bit is vali of the star server trous	2 o o ks (trus stati it sumpte traine req	int priority bit-1	int priority bit-0	int status
		ib y iw olioi	en. Peoly	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
		0	MCR	0 8	0 0	0	loop back	OP2*	OP1*	RTS*	DTR*
1		6. 1 16	LSR A	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1	1	1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

DLL and DLM are accessible only when LCR bit-7 is set to "1".

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REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C450 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2¹⁶-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:

0=disable the receiver ready interrupt. 1=enable the receiver ready interrupt.

IER BIT-1:

0=disable the transmitter empty interrupt. 1=enable the transmitter empty interrupt.

IER BIT-2:

0=disable the receiver line status interrupt. 1=enable the receiver line status interrupt.

IER BIT-3:

0=disable the modem status register interrupt. 1=enable the modem status register interrupt.

IER BIT 7-4:

All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C450 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C450 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

Р	D2	D1	D0	Source of the interrupt
1	10	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

1=no interrupt pending.

ISR BIT 1-2:

Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:

These bits are not used and are set to "0".

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
. 0	1	6
1	0	7 3 5 1 18 1
1	1	an last a 8 source evers

LCR BIT-2:

The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1,000	5 000 5	1-1/2
- 1 _{enti}	6,7,8	2

LCR BIT-3:

Parity or no parity can be selected via this bit.

1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.

0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.

1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:

If the parity bit is enabled, LCR BIT-5 selects the forced parity format. LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data. LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:

Break control bit. It causes a break condition to be transmitted (the TX is forced to low state). 0=normal operating condition.

1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:

The internal baud rate counter latch enable (DLEN). 0=normal operation. 1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:

0=force DTR* output to high. 1=force DTR* output to low.

MCR BIT-1:

0=force RTS* output to high. 1=force RTS* output to low.

MCR BIT-2:

0=set OP1* output to high. 1=set OP1* output to low.

MCR BIT-3:

0=set OP2* output to high. 1=set OP2* output to low.

MCR BIT-4:

0=normal operating mode.

1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode, the receiver and transmitter interrupts

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are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:

Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:

0=no data in receive holding register 1=data has been received and saved in the receive holding register.

LSR BIT-1:

0=no overrun error (normal).

1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:

0=no parity error (normal).

1=parity error, received data does not have correct parity information.

LSR BIT-3:

0=no framing error (normal).

1=framing error received, received data did not have a valid stop bit. In

LSR BIT-4:

0=no break condition (normal).

1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:

0=transmit holding register is full. ST16C450 will not accept any data for transmission.

1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6: on misborn of betgannon and 1940 bris

0=transmitter holding and shift registers are full. 1=transmitter holding and shift registers are empty.

LSR BIT-7: (MOLE RETRIEDED JONTHOS BINL

Not used. Set to "0".

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:

Indicates that the CTS* input to the ST16C450 has changed state since the last time it was read.

MSR BIT-1:

Indicates that the DSR* input to the ST16C450 has changed state since the last time it was read.

MSR BIT-2:

Indicates that the RI* input to the ST16C450 has changed from a low to a high state.

MSR BIT-3:

Indicates that the CD* input to the ST16C450 has changed state since the last time it was read.

MSR BIT-4:

This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:

This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:

This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7: Monthly of beatstening at white GCO*9

This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C450 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	1

ST16C450 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE		
IER	IER BITS 0-7=0		
ISR	ISR BIT-0=1, ISR BITS 1-7=0		
LCR	LCR BITS 0-7=0		
MCR	MCR BITS 0-7=0		
LSR	LSR BITS 0-4=0,		
	LSR BITS 5-6=1 LSR, BIT 7=0		
MSR	MSR BITS 0-3=0,		
	MSR BITS 4-7=input signals		



SIGNAL	RESET STATE			
TX	High			
OP1*	High			
OP2*	High			
RTS*	High			
DTR*	High			
INT	Low			

AC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
0-0-1	Clock high pulse duration	Page				BLE (1.8432 MHz C
T ₁	Clock High pulse duration	50	-0.7		ns	Note: 2
T ₂	Clock low pulse duration	50	- 7		ns	Note: 2
T ₃	Clock lise/fall tillle			10	ns	San I have a selective
T ₄	Daud out rise/fail tillle		яоля	100	ns	100 pF load
T_{2}^{2} T_{3}^{4} T_{5}^{4} T_{6}^{7} T_{7}^{8} T_{10}^{9}	Address strobe width	30			ns	
T ₆	Address setup time	15			ns	4.5
T ₇	Address hold time	15		- 11 1	ns	50
T ₈	Chip select setup time	5	200		ns	(A)
T ₉	Chip select hold time	0	10.28		ns	The second second
T ₁₀	CSOUT delay from chip select		8201	10	ns	134.5
T,,	IOR* to DDIS* delay			35	ns	100 pF load
T ₁₂	Data setup time	15			ns	Note: 1
13	Data hold time	15	1		ns	Note: 1
T.,	IOW* delay from chip select	10	1		ns	Note: 1
T ₄₅	IOW* strobe width	55	V- 3		ns	2400
T ₁₆	Chip select hold time from IOW*	0			ns	Note: 1
T ₁₇	Write cycle delay	55			ns	0084
Tw	Write cycle=T ₁₅ +T ₁₇	105			ns	7200
T ₁₉	Data hold time	15			ns	0086
T.,	IOR* delay from chip select	25			ns	Note: 1
T ₂₁ T ₂₃	IOR* strobe width	65	13-71-31		ns	88.4K
T.,	Chip select hold time from IOR*	0	77.3		ns	Note: 1
T ₂₄ T ₂₅	Read cycle delay	55			ns	115.2K
Tr	Read cycle=T ₂₃ +T ₂₅	115			ns	
T ₂₆	Delay from IOR* to data	25			ns	100 pF load
T ₂₈	Delay from IOW* to output			50	ns	100 pF load
T ₂₉	Delay to set interrupt from MODEM			70	ns	100 pF load
29	input				110	, co pr road
T ₃₀	Delay to reset interrupt from IOR*			70	ns	100 pF load
T ₃₁	Delay from stop to set interrupt				*	100 pF load
T ₃₂	Delay from IOR* to reset interrupt		There I	1 _{Rclk} 200	ns	100 pF load
T ₃₃	Delay from initial INT reset to transmit	8	1	24	*	100 pr load
33	start	Ü		24		

3

AC ELECTRICAL CHARACTERISTICS

 $T_{\Delta}=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
T ₃₄ T ₃₅ N	Delay from stop to interrupt Delay from IOW* to reset interrupt Baud rate devisor	1	gan	100 175 2 ¹⁶ -1	ns ns	

Note 1: Applicable only when AS* is tied low. Note 2: 1.8432 Mhz crystal or External clock.

* = Baudout* cycle

36 N.C. D5 2 35 RESET 3 34 D6 OP1* 33 D7 5 32 RTS* RCLK 6 31 N.C. ST16C450CQ48 30 8 29 TX N.C 9 CS0 28 AO 10 27 A1 CS1 CS2* 11 26 A2 12 25 N.C. BAUDOUT* TAL1
TAL2
IOW
IOW
IOR*
IOR*
IOR*

ABSOLUTE MAXIMUM RATINGS

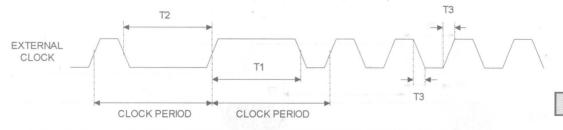
Supply range Voltage at any pin Operating temperature Storage temperature Package dissipation 7 Volts GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

DC ELECTRICAL CHARACTERISTICS

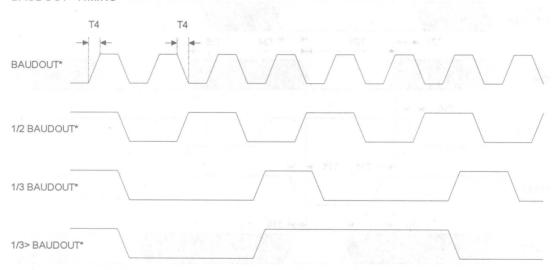
 $T_A=0^{\circ}$ - 70 C, Vcc=5.0 V ± 10% unless otherwise specified.

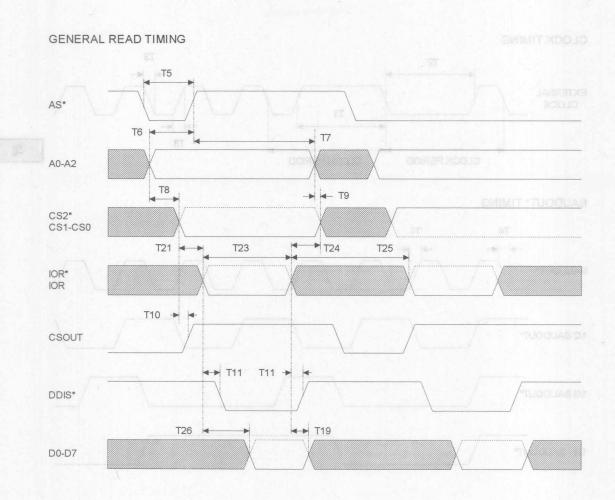
Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
V _{II CK}	Clock input low level	-0.5		0.6	V	
V _{ILCK}	Clock input high level	3.0		VCC	V	C13-5 - 58-1
V	Input low level	-0.5		0.8	V	
V _{IL} V _{IH}	Input high level	2.2		VCC	V	
Vol	Output low level on all outputs			0.4	V	I _{oL} = 6 mA
V _{OL}	Output high level	2.4			V	I _{OH} = -6 mA
Icc	Avg. power supply current	4	6		mA	On
I	Input leakage	1 2 8 2	2 2 5	±10	μА	
ICL	Clock leakage		CHENT	±10	μА	

CLOCK TIMING

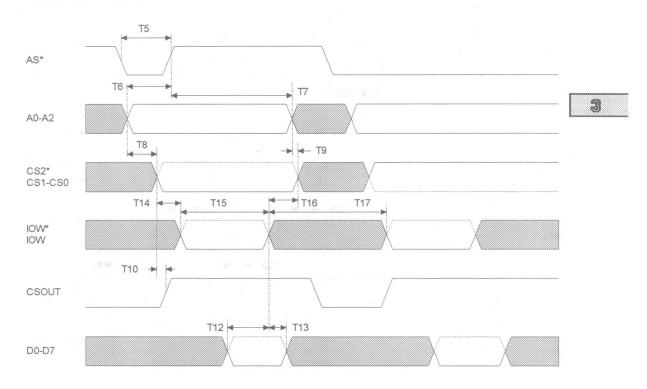


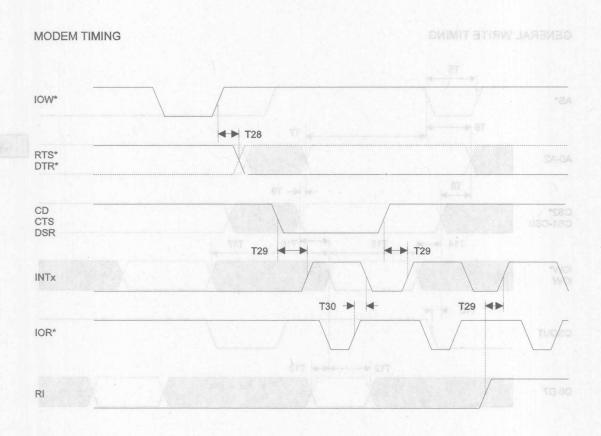
BAUDOUT* TIMING

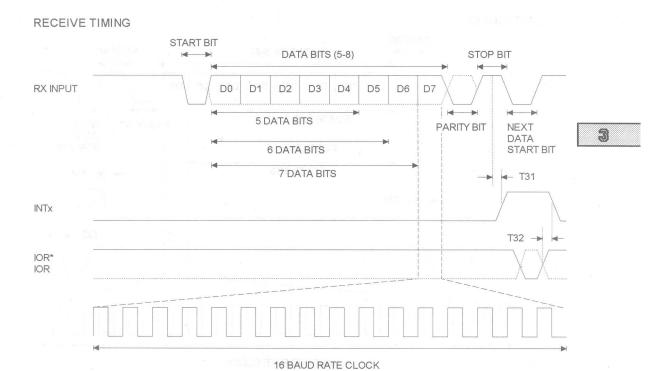


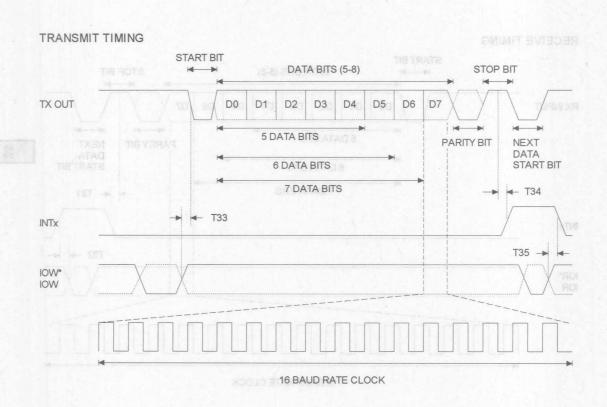


GENERAL WRITE TIMING











ST16C1450 ST16C1451

Printed September 6, 1994

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

DESCRIPTION

The ST16C1450/51 is a universal asynchronous receiver and transmitter. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C1450/51 is an improved version of the SSI 73M1550 and SSI 73M2550 UART with higher operating speed and lower access time. The ST16C1450/51 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C1450/51 provides internal loop-back capability for on board diagnostic testing.

The ST16C1450/51 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

FEATURES

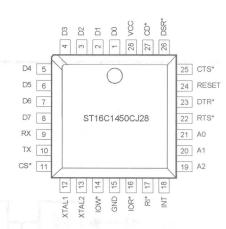
- Pin to pin and functional compatible to SSI 73M1550/2550
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Software compatible with INS8250, NS16C550
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source
- 28 Pin plastic-Dip and PLCC package
- Pin-to-pin compatible to ST16C1550/1551

ORDERING INFORMATION

Part number	Package C	perating	temperature
ST16C1450CP28	Plastic-DIP	0° C	to + 70° C
ST16C1450CJ28	PLCC	0° C	to + 70° C
ST16C1450CQ48	TQFP	0° C	to + 70° C
ST16C1451CP28	Plastic-DIP	0° C	to + 70° C
ST16C1451CJ28	PLCC	0° C	to + 70° C
ST16C1451CQ48	TQFP	0° C	to + 70° C

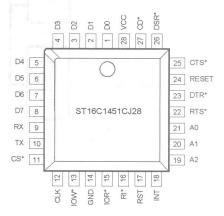
*Industrial operating range are available.

ST16C1450 PLCC Package



3

ST16C1451 PLCC Package

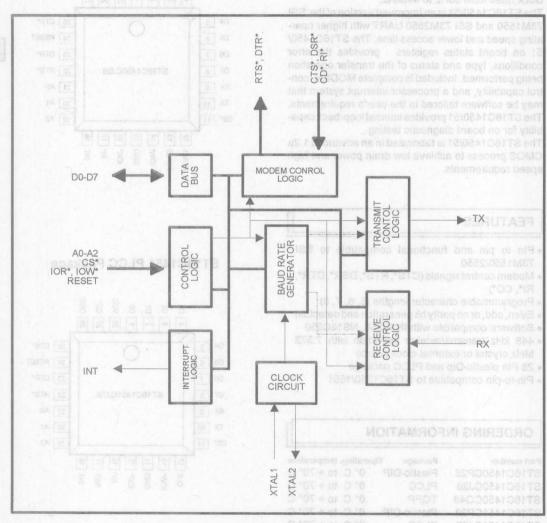




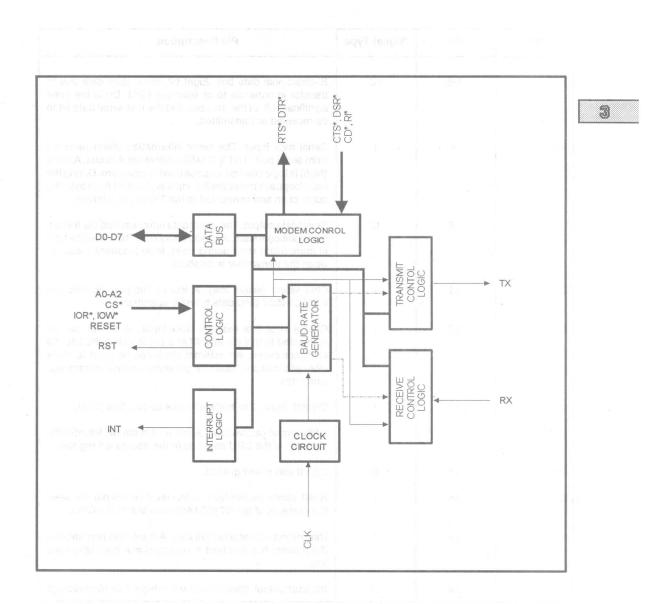
UNIVERSAL ASYNCHRONOUS RECEIVERTRANSMITTER

ST16C1450 BLOCK DIAGRAM

The ST16C145C/51 is a universal asynchronous reselver and transmitter. A programmable baud rate generator is provided to select transmit and raceive



ST16C1451 BLOCK DIAGRAM



ST16C1450 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description			
D0-D7	1-8	1/0	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.			
RX 9			Serial data input. The serial information (data) received from serial port to ST16C1450 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally. Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.			
		0				
CS*	11	888 11	Chip select (active low). A low at this pin enables the ST16C1450 / CPU data transfer operation.			
XTAL1	12	1	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.			
XTAL2	13		Crystal input 2 or buffered clock output. See XTAL1.			
IOW*	14	1	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.			
GND	15	0	Signal and power ground.			
IOR*	16	1	Read strobe (active low). A low level on this pin transfers the contents of the ST16C1450 data bus to the CPU			
RI*	17	1	Ring detect indicator (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.			
INT	18	0	Interrupt output. (three state / active high) This pin goes high			

ST16C1450 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description			
	dels en off find und I URC set over the try and become		(when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.			
A0-A2	21-19	I	Address select line. To select internal registers.			
RTS* A Rigory Manager JCL or Manager annul Grantesto	himanada seco	o or a side and a	Request to send (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.			
DTR* som alts	dgool (23) taes	n) srato Paing a manufler to u.so. .cactives fovol. A 7 CF u data nov				
	24 w nig sint ne wa		Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.			
CTS*	entino evol wa	the CPU cate to I power ground. e (astroclow): 4	Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR bit-4. CTS* has no effect on the transmit or receive operation.			
	26	s of the ST (SC) indicator (Scriver)	Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.			
		ut (active high). set output which i				
VCC	28		Power supply input.			

ST16C1451 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description				
amider empty,		I/O v1 be selected to the control of	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.				
RX Himselem entre material entre material entre minimal en	9 indicate the hills pin ill set this pin set to high. No	I (wol avilos) base	Serial data input. The serial information (data) received from serial port to ST16C1451 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.				
TX ndicate that	10 oT ./wol	o nal read (active is ready to race)	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.				
CS*Jottuquo 1	III se ll e DTR te after with	at the I (CR bit-1 w be set to high sta far the reset. Note	Chip select (active low). A low at this pin enables th ST16C1451 / CPU data transfer operation.				
CLK	rango 12 leos	n the transmit of m t (active High). A nic	External clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.				
	00113	r input will be dila	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.				
GND	14	Hun in ot whose a	Signal and power ground.				
IOR*	15	apolished.	Read strobe (active low). A low level on this pin transfers the contents of the ST16C1451 data bus to the CPU.				
RI*	16	gradoxe (fyber) ve any effect on th	Ring detect indicator (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.				
RST astsolbni ili		of (sof or low). A been detected by a livingut.	Reset output (active high). The ST16C1451 provides a buffered reset output which is gated internally with MCR bit-2.				

ST16C1451 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INT	18		Interrupt output. (three state / active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
A0-A2	21-19	15 B 0 DW	Address select line. To select internal registers.
RTS*	22	0	Request to send (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	23	0	Data terminal read (active low). To indicate that ST16C1451 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
RESET	24	1	Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	25	1	Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR*	26		Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD*	27	1	Carrier detect (active low). A low on this pin indicates the carrier has been detected by the modem.
VCC	28	1	Power supply input.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0 11	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	on o all Tr	rent 1 vits	Interrupt output, (firree state) a	Line Control Register
Teve 1	0	0	(wiren enabled by the intenuor	Modem Control Register
1	0	eld fliev	Line Status Register	
1	1 at	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0	Address select tine. To select	LSB of Divisor Latch
0	0	1		MSB of Divisor Latch
Integral	ailt tedt à	million of	Dumi outlied three of teaming	

All unused input pins should be tied to VCC or GND.

		- 52
ST16C1451 is ready to reseive date. This pin can be		
in in & . Opposite the madem common register (MCR bit-0).		
4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4		
register or after the 1 O 1 an that this pin does not have	36 N.C.	
anolisago oviso N.C. 2 isosti atti no toelta yns.	35 N.C.	
D4 3	34 CTS*	
Masterraset (active high 4 to this pin will raset all the		
one fueling setting and the free state of the state of th	33 RESET	
entit receiver input will beld so beld so set time.	32 DTR*	
D7 6 ST16C1450CQ48	31 RTS*	
MECOM e el langie 1870 (RX 7 of systes) in ST16C1451CQ48	30 A0	
MIDUODITE STRINGS TO LO EM LA OF SVINGS) DIGGE OF RESID		
control function input w xrconditions can be tested by	29 N.C.	
Amanali offino iselfe on aa cs* 9. A-TIE Rall onforbase	28 A1	
N.C. 10 NGRS18QO EVISOOT TO	27 A2	
N.C. 11		
Data set ready (active k 12 No. on this pln indicates the	26 N.C.	
nio aint THAU niiw sisbe de la	25 N.C.	
7		
N.C. N.C. XTAL1 IOW* N.C. N.C. GND IOW* R.S.T. R.S.T. R.S.T. R.S.T. N.C. N.C. N.C. N.C. N.C. N.C. N.C. N		
The Carrier detect (active low). A low on this pin indicates the		

ST16C1450 ACCESSIBLE REGISTERS

A2 A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0	0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0	1.	IER visc	e Okaba Buya Buya Buya Buya Buya Buya Buya Buy	2	0/ special mode	0 0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1	0	ISR to	0 0	0 0	0 0	0 0	0 0	int priority bit-1	int priority bit-0	int status
0 1	1	CALCR GOTO	divisor latch enable	set break	set parity	even parity	parity	stop bits	word length bit-1	word length bit-0
1 0	0	MCR	0/power down	oop 0 sek e	0 0	loop back	INT enable	SOFT reset	RTS*	DTR*
/1 0 6/30 (0/8)	1nu	LSR/ins	0000	trans. empty	trans. holding empty	break interrupt	framing	parity error	overrun error	receive data ready
1-1	0	MSR	CD	RISTS	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1	1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0	0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0	1 0	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

DLL and DLM are accessible only when LCR bit-7 is set to "1".

ST16C1451 ACCESSIBLE REGISTERS

A2 A1 A	0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	6 bit-1	bit-0
0 0 0	0	III THR SHO	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
noddin		tell IER vied line hold fatus regit etrupt	tatus emupt s	2	0/ special mode	0 0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 (O I	al ISR milional whom	0 0	0 0	0 0	0 0	0 0	int priority bit-1	int priority bit-0	int status
		W LCR quie nel and hd	divisor latch enable	set break	set parity	even parity	parity	stop stop bits	word length bit-1	word length bit-0
100	0	MCR 10	0/power down	0000 0000	0 0	loop back	INT enable	SOFT	MRTS*	DTR*
100 steb		LSR me	O hios	trans. empty	trans. holding empty	break interrupt	framing	parity error	overrun error	receive data ready
a1sl1 (0	MSR	CD	RIFTO	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1111	1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	8 bit-1	bit-0
000	0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
00	1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

DLL and DLM are accessible only when LCR bit-7 is set to "1". Accesses the MLG bots 11G

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C1450/51 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2¹⁶-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:

0=disable the receiver ready interrupt. 1=enable the receiver ready interrupt.

IER BIT-1:

0=disable the transmitter empty interrupt. 1=enable the transmitter empty interrupt.

IER BIT-2:

0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:

0=disable the modern status register interrupt. 1=enable the modern status register interrupt.

IER BIT-5:

0=normal ST16C450 mode. 1=special mode. Enable power down and SOFT rest.

IER BIT 4,6-7:

All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C1450/51 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C1450/51 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority levels

Р	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data
3	0	1	0	Ready) TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modern Status Register)

ISR BIT-0:

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

1=no interrupt pending.

ISR BIT 1-2:

Logical combination of these bits, provides the highest priority interrupt pending.

ISR bit 3-7:

Not used as a more assistant to the control of the

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2: MIGJON BVIBOS R OMA TIMEMASTI

The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	His (1HT)
art 1	5 5 6	1-1/2
111	6,7,8	2

LCR BIT-3: 2 moleneco sinw a faiti sinti nelsigat

Parity or no parity can be selected via this bit.

1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4: The life time and to work little at XSI and the

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.

0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.

1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5: Met No eldisque al militaristante de la A

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.

LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:

Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).

0=normal operating condition.

1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:

The internal baud rate counter latch enable (DLEN). 0=normal operation.

1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:

0=force DTR* output to high. 1=force DTR* output to low.

MCR BIT-1:

0=force RTS* output to high. 1=force RTS* output to low.

MCR BIT-2:

0=normal operation.
1=software reset, set RST output to high.

MCR BIT-3:

0=set INT output pin to three state mode.
1=set INT output pin to normal operation mode.

MCR BIT-4:

0=normal operating mode.

1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, SOFT reset and INT enable are connected to modem control inputs.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-6:

Not used. Are set to zero permanently.

MCR bit-7:

0=normal mode.

1=power down mode. XTAL1, XTAL2, and baud rate generators are disabled.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:

0=no data in receive holding register 1=data has been received and saved in the receive holding register.

LSR BIT-1:

0=no overrun error (normal).

1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:

0=no parity error (normal).

1=parity error, received data does not have correct parity information.

LSR BIT-3:

0=no framing error (normal).

1=framing error received, received data did not have a valid stop bit.

LSR BIT-4:

0=no break condition (normal).

1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:

0=transmit holding register is full. ST16C1450/51 will not accept any data for transmission.

1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6: did deser 1 50 s of the Lavit

0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:

Not used



MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:

Indicates that the CTS* input to the ST16C1450/51 has changed state since the last time it was read.

MSR BIT-1:

Indicates that the DSR* input to the ST16C1450/51 has changed state since the last time it was read.

MSR BIT-2:

Indicates that the RI* input to the ST16C1450/51 has changed from a low to a high state.

MSR BIT-3:

Indicates that the CD* input to the ST16C1450/51 has changed state since the last time it was read.

MSR BIT-4:

This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:

This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:

This bit is equivalent to SOFT reset in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:

This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C1450/51 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	esoftware rese
75	1536	
110	1047	0.026
150	768	thing Till least
300	384	unituo Tid. Ioawi
600	192	
1200	96	LTIS ROS
2400	48	sheep lamages
3600	32	spot sidense
4800	24	chio rettimanan
7200	16	ne receiver inclu
9600	12	disabled intern
19.2K	6	and of beiner
38.4K	3	ne TM breatean
56K	2	2.77
115.2K	nd bos 141/2007 a	n this mode

ST16C1450/51 EXTERNAL RESET CONDITION

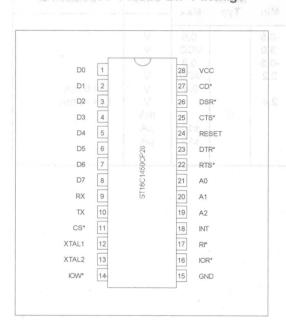
REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0,
en burnel have 8	LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0,
	MSR BITS 4-7=input signals

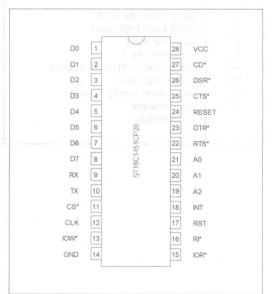
SIGNALS	RESET STATE
TX	High
SOFT reset	High
RTS*	High
DTR*	High
INT	Three state mode

3

ST16C1450 Plastic-DIP Package

ST16C1451 Plastic-DIP Package





ABSOLUTE MAXIMUM RATINGS

Supply range Voltage at any pin Operating temperature Storage temperature Package dissipation 7 Volts GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

DC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70° C, $V_{CC}=5.0 \text{ V} \pm 10\%$ unless otherwise specified.

Symbol	Parameter	Min	Limits Typ Ma	Units	Conditions
VILCK	Clock input low level	-0.5	0.	6 V	
VIHCK	Clock input high level	3.0	VC	CV	
VIL	Input low level	-0.5	0.	8 V	
V _{IH}	Input high level	2.2	VC	CV	P 60
Vol	Output low level on all outputs		0.	4 V	I _{oL} = 6 mA
V _{OH}	Output high level	2.4	*xied	V	I _{OH} = -6 mA
I _{cc}	Avg. power supply current		6	mA	III eg
I	Input leakage		±1	0 μΑ	2 20
ICL	Clock leakage		±1	0 μΑ	

AC ELECTRICAL CHARACTERISTICS

 T_{Δ} =0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
T.	Clock high pulse duration	50			ns	Note: 1
Τ'	Clock low pulse duration	50			ns	Note: 1
T.	Clock rise/fall time			10	ns	1,1010. 1
T ₁ T ₂ T ₃ T ₈ T ₉ T ₁₂	Chip select setup time	5			ns	
Ť	Chip select hold time	0	57	T.	ns	
T ⁹	Data setup time	15			ns	
T ₁₃	Data hold time	15			ns	
T ₁₄	IOW* delay from chip select	10			ns	
T ₁₅	IOW* strobe width	50			ns	
T ₁₆	Chip select hold time from IOW*	0	p-	217	ns	
T ₁₇	Write cycle delay	55	19		ns	
Tw	Write cycle=T ₁₅ +T ₁₇	105	1 1		ns	
T ₁₉	Data hold time	15		Mary Line 2013	ns	151 5 A.E.
T 19	IOR* delay from chip select	10			ns	
T ₂₁ T ₂₃ T ₂₄ T ₂₅ Tr	IOR* strobe width	65			ns	
T 23	Chip select hold time from IOR*	0			ns	
T ²⁴	Read cycle delay	55	1			
Tr 25	Read cycle delay Read cycle=T ₂₃ +T ₂₅	105			ns	
T	Delay from IOR* to data	105		25	ns	100 pF lood
T ₂₆ T ₂₈				35	ns	100 pF load
28	Delay from IOW* to output			50	ns	100 pF load
T ₂₉	Delay to set interrupt from MODEM input			70	ns	100 pF load
T ₃₀	Delay to reset interrupt from IOR*			70	ns	100 pF load
T ₃₁	Delay from stop to set interrupt			1 _{Rclk}	*	100 pF load
T ₃₂	Delay from IOR* to reset interrupt			200	ns	100 pF load
T ₃₁ T ₃₂ T ₃₃	Delay from initial INT reset to transmit start	8		24	*	
T ₃₄	Delay from stop to interrupt		7.	100	ns	
T ₃₅	Delay from IOW* to reset interrupt	100		175	ns	
N	Baud rate devisor	1		216-1		

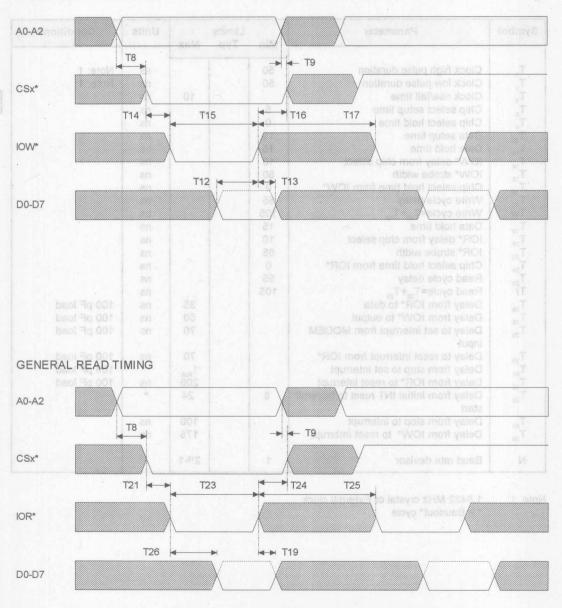
Note 1:

1.8432 MHz crystal or External clock

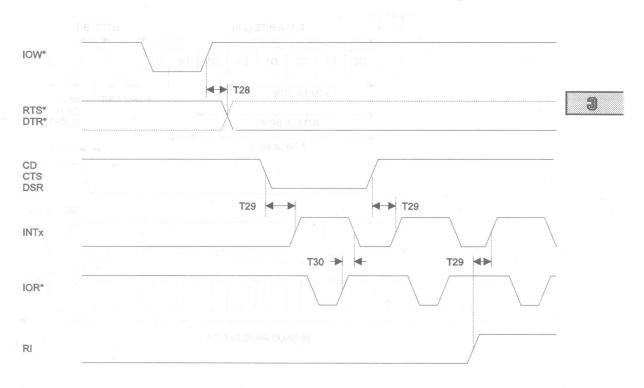
* = Baudout* cycle

AC ELECTRICAL CHARACTERISTICS

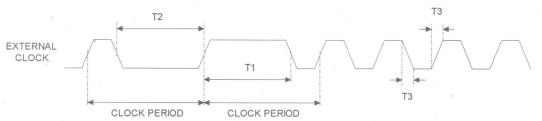
GENERAL WRITE TIMING



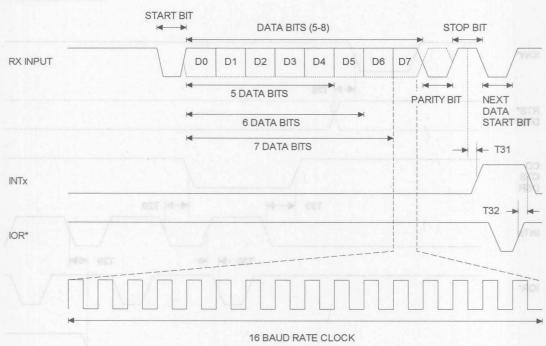
MODEM TIMING

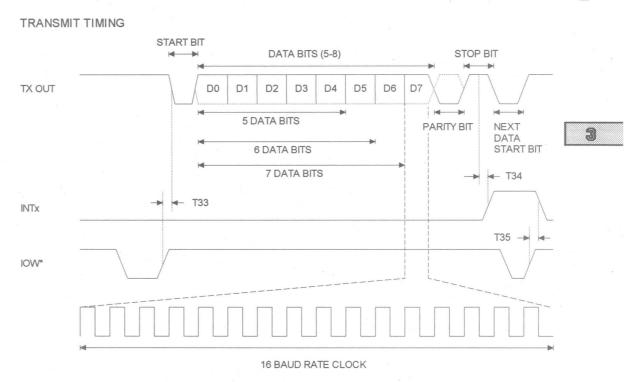


CLOCK TIMING

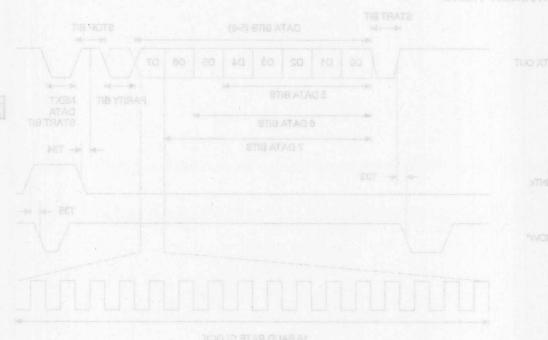








TRANSMIT TIMBUAST





ST16C2450

Printed September 6, 1994

DUAL UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

DESCRIPTION

The ST16C2450 is a dual universal asynchronous receiver and transmitter. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50Hz to 448kHz for each UART section.

The ST16C2450 is an improved version of the NS16C450 UART with higher operating speed and lower access time. The ST16C2450 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C2450 provides internal loop-back capability for on board diagnostic testing.

The ST16C2450 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

FEATURES

- Functional compatible to NS16450, VL16C450, WD16C450
- Modern control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- · Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

ORDERING INFORMATION

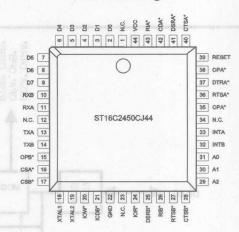
 Part number
 Package
 Operating temperature

 ST16C2450CP40
 Plastic-DIP
 0° C to + 70° C

 ST16C2450CJ44
 PLCC
 0° C to + 70° C

*Industrial operating range are available

PLCC Package



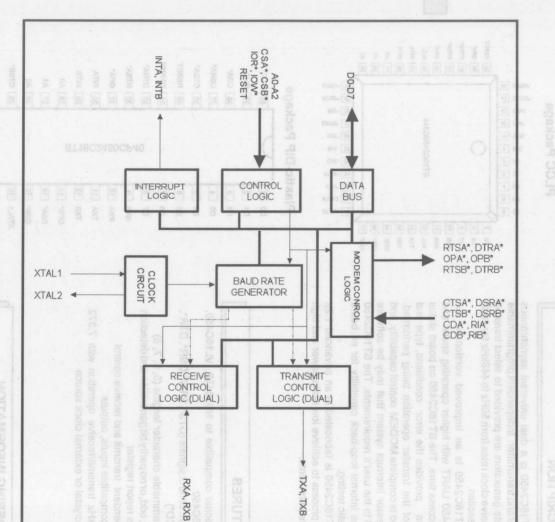
Plastic-DIP Package



21 IOR*

GND 20

BLOCK DIAGRAM



3-46

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
		able o OVI il (eciv it pin is set to the ris angebied via CP R bit-3).	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
	send. Writing a bit-1) will set tills will be set to hig	send Al 3 (active) as data ready to pay the polister (MCR) he read this plu on have any of e	Serial data input A/B. The serial information (data) received from serial port to ST16C2450 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B ndicate that gin can be MOR bib-0).	ive data. This order register (o at ready A/S (to is ready to rete is the modern a	Serial data output A/B. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
	14,15		Chip select A/B. (active low) A low at this pin enables the ST16C2450 / CPU data transfer operation.
output and the time.	16 Il winiq alal no de The transmitter also gunng rede	I (active bigh) A liii internal registers ringut will be dida	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	t bnoo e17riw n	al evitos). Ex bin atral fulction ino	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	ding the MSR BIT eceive Iperation	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	A J row 21 bags	dy AJB (active low is read I to exchan se any effect on th	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C2450 data bus to the CPU.
A0-A2	28-26	1	Address select lines. To select internal registers.
INT A/B	wol A (wol avii	as bee Outlected Indicator AVB (sc	Interrupt output A/B. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
		data Ous. Eight inhalion to or fro it of the data but or transmitted.	Interrupt enable output (active low). This pin stays high when INT out pin is set to three state mode and goes low when INT pin is enabled via OP2*. See bit-3 modem control register (MCR bit-3).
roult. A mark o. During fire from external stemally.	receive input of (low) is logic zerous to disabled the TX output in	put A OThese on to ST18C245 on to ST18C245 on to ST18C245 on the RX in the RX ind connected to	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
s. Vir*B\A.STC cal loopbask s enables line	id vir 33,34 go pl., seen graub beidselb er s ig eidt te wot A nottsrego set	butput A/B. The additio OI stant, at the tenth of the transmit A/B. (active low). A/B. (active low). A/B. (active low).	Data terminal ready A/B (active low). To indicate that ST16C2450 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
RESET in ent e	ALZ p 25 o utiliza	I f or external di othis pili and XI ouit. An external ill and baud rate p	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
	w on this pin w	it 2 or buffered of (active low) A to the CPU date bus	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR A/B*	37,22 sint no level wo to data bus to t	I s. (active low) A is of the ST16C24	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD A/B*	38,19 (dp) This pin go	ect lines. To sell out A/B. (active a the interrupt one	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
	39,23	reserver data av receiver data av us condition Rag	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.

SYMBOL DESCRIPTION

Symbol		Pin	Signal T	уре		Pin	Descripti	on		
CC 0-lid	f-tid	40 gajid	E-tid	≱ dP	ower supp	ly input.		ЯНТ		
ND I	ransitilt i	20	mebcO ₁	S	ignal and p	ower gro	und.			
egister	register. r	status itemupt	interrupt in							
						0				
brow dength 0-tid					set parity					
						0				
OGRA	MMING	TABLE								
A2	A1	A0	READ MO	DE		WRITE	MODE		0	
0	0 1 1	0 1 A 1 0 S-1d	Receive H			Interru	nit Holding ot Enable F	Register	1.1	
0	0 0	0 2-10	Line Statu	N-Md	6-110		ontrol Regi Control R		0	
8 ₁ ma.	1 1	0 0 mid	Modem St Scratchpa	atus Regi	ster	Scratch	npad Regis	MAG ter	1	
0	0	0			LCR bit	LSB of	Divisor La		and a	

ST16C2450 ACCESSIBLE REGISTERS A/B

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	IER	0	0	n bn o lan	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0	1	0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0	1	1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1	0	0	MCR	0	0	0	loop back	OP2/ INT enable	Not used	RTS*	DTR*
1	0	1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	CD	RI	DSR	стѕ	delta CD*	delta RI*	delta DSR*	delta CTS*
1	1	1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
.0	0	1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS A/B

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C2450 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2¹⁶ -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modern status registers to the INT output pin.

IER BIT-0:

0=disable the receiver ready interrupt.

IER BIT-1:

0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:

0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:

0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

The Line Control Register is used to:7-4 TIR RILL

All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C2450 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C2450 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

Ρ	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status Register)
2	1	0	0	RXRDY (Received Data Ready)
3	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modem Status Register)

ISR BIT-0:

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

1=no interrupt pending.

ISR BIT 1-2; gurietni ytume leftimanaut ent eidense)

Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7: umotal autota enil neviscen enil aldenas t

These bits are not used and are set to "0".

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0 0	nios ene al 5 um ami ner
0	niwallot s	att "bealvi6" ei laume
1	0	demupt le 7 els:
1	1	8

LCR BIT-2:

The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)		
0	5,6,7,8	FIXE 10		
1	5	1-1/2		
phiblo	6,7,8	2		

LCR BIT-3: PANGLICH SYLBORS GVA TIMEMAST

Parity or no parity can be selected via this bit. 0=no parity

1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4: \$1000 srft retenant like (FIHT) reteiper ainti

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.

0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.

1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5: size of T. fid hate of to remode all at northweet

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.

LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6: MAD STAR QUAS SUBAMMARDORS

Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).

0=normal operating condition.

1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7: neo sets 9 bus 8 scimotzu0. (ets 9 bus 8 x

The internal baud rate counter latch enable (DLEN). 0=normal operation.

1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:

0=force DTR* output to high. 1=force DTR* output to low.

MCR BIT-1:

0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:

not used except in local loop-back mode.

MCR BIT-3:

0=set INT output pin to three state mode and OP2* output to high.

1=set INT output pin to normal operating mode and OP2* output to low.

MCR BIT-4:

0=normal operating mode.

1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and OP2*/INT enable are connected to modem control inputs.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:

Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:

0=no data in receive holding register
1=data has been received and saved in the receive holding register.

LSR BIT-1:

0=no overrun error (normal).

1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:

0=no parity error (normal).

1=parity error, received data does not have correct parity information.

LSR BIT-3: at T2 will of fugal "GO will be it setsoible

0=no framing error (normal). - 11 90012 01812 bendant

1=framing error received, received data did not have a valid stop bit. In

LSR BIT-4: a fremilgmoo entrei if sebom pland-good

0=no break condition (normal).

1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5: a memiligraco edit al fl. ebom xbad-gool

0=transmit holding register is full. ST16C2450 will not accept any data for transmission.

1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:

0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty.

LSR BIT-7:

Not used. Set to "0".

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:

Indicates that the CTS* input to the ST16C2450 has changed state since the last time it was read.



MSR BIT-1:

Indicates that the DSR* input to the ST16C2450 has changed state since the last time it was read.

MSR BIT-2:

Indicates that the RI* input to the ST16C2450 has changed from a low to a high state.

MSR BIT-3:

Indicates that the CD* input to the ST16C2450 has changed state since the last time it was read.

MSR BIT-4:

This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:

This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input: WORKSONTE HIM ENGINEER PRIDER MADE AND ALL OF THE PRIDER PRI

MSR BIT-6:30 .vigme at retainer publich timenant=1

This bit is equivalent to MCR bit-2 during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7: ereisiner flids bas publical retires = 7-TIB RSM

This bit is equivalent to OP2*/INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SIGNALS	RESET STATE
wheneviXTa	t" (High one stid eas
OP2*	one High I3GOM and m
	be High O edt revens
DTR*	High
INT	Three state mode

SCRATCHPAD REGISTER (SR)

ST16C2450 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR		
ons abom priori	2001	set INT output 2° output to lo		
	1536	or major a		
		0.026		
	857 om or			
) sho 768 sd-qc			
	dpid 1:384 (XT)			
	920 1920 XS			
	o estim96 enterty			
2400	179 1948 bosh	he receiver in		
3600	belos 3200 ers	2"/INT enable		
4800	24	uts.		
7200	neceived trans			
	mebo12arlT Ja			
19.2K	nel, but 8he intern	also operation		
	bits of 118 Moden			
56K	Modem (Sontrolling	100 2.77 best		
115.2K	by the TER.	t ellorinos Illia		

ST16C2450 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE			
dER tenent etab	IER BITS 0-7=0 void relation a			
ISR	ISR BIT-0=1, ISR BITS 1-7=0			
LCR	LCR BITS 0-7=0			
MCR	MCR BITS 0-7=0			
LSR	LSR BITS 0-4=0,			
d in the receive	LSR BITS 5-6=1 LSR, BIT 7=0			
MSR	MSR BITS 0-3=0, repriner prilb			
	MSR BITS 4-7=input signal			

AC ELECTRICAL CHARACTERISTICS

 $T_{\rm A}$ =0° - 70° C, Vcc=5.0 V \pm 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
T ₁ T ₂ T ₃ T ₈ T ₉ T ₁₂ T	Clock high pulse duration	50	mes	HABIT	ns	TAMOTOR IN
T.	Clock low pulse duration	50	(mass)		ns	External clock
T.	Clock rise/fall time	Biomen	szionanii	10	ns	0° - 70° C. Voc=8.0
T.	Chip select setup time	15	DETANGE IN	A GREATH DO	ns	N. O O O O O O O O
T.	Chip select hold time	0			ns	
T,	Data set up time	15		1916	ns	today
T,2	Data hold time	15			ns	
T ₁₃ T ₁₄	IOW* delay from chip select	10			ns	
T,5	IOW* strobe width	50			ns	V Clock inpu
T ₁₆	Chip select hold time from IOW*	0		1	ns	LICK Clock in but
T ₁₇	Write cycle delay	55	100		ns	i wet brant lew t
Tw	Write cycle=T ₁₅ +T ₁₇	105			ns	dairt tront
T ₁₉	Data hold time	15		intuo lii	ns	V Output low
T ₂₁	IOR* delay from chip select	10		erdeans and	ns	alif luciuO
T ₂₃	IOR* strobe width	65		Insm	ns	lawag pvA
T ₂₄	Chip select hold time from IOR*	0		21.150.1-0	ns	blael fugni
T ₂₅ Tr	Read cycle delay	55			ns	L Clock leak
Tr	Read cycle=T ₂₃ +T ₂₅	115			ns	
T ₂₆ T ₂₈	Delay from IOR* to data			35	ns	100 pF load
T ₂₈	Delay from IOW* to output			50	ns	100 pF load
T ₂₉	Delay to set interrupt from MODEM input			70	ns	100 pF load
T ₃₀	Delay to reset interrupt from IOR*	-		70	ns	100 pF load
T ₃₁	Delay from stop to set interrupt			1 _{Rclk}	ns	100 pF load
32	Delay from IOR* to reset interrupt			200	ns	100 pF load
T ₃₃	Delay from initial INT reset to transmit start	8		24	*	
T ₃₄	Delay from stop to interrupt			100	ns	
T ₃₅	Delay from IOW* to reset interrupt	-		175	ns	
N	Baud rate devisor	1		216-1		
		*				

Note 1: * = Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

Supply range Voltage at any pin Operating temperature Storage temperature Package dissipation 7 Volts
beliceds sciwned assign 201 GND-0.3 V to VCC+0.3 V
0° C to +70° C
-40° C to +150° C
500 mW

DC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter		_imits Typ Max	Units	Conditions
VILCK VIHCK VIH VOL VOH ICC IIL ICL	Clock input low level Clock input high level Input low level Input high level Output low level on all outputs Output high level Avg power supply current Input leakage Clock leakage	-0.5 3.0 -0.5 2.2 2.4	0.6 VCC 0.8 VCC 0.4 6 ±10 ±10	V V V V MA µA µA	I _{OL} = 6 mA I _{OH} = -6 mA

Telegy from IOW* to output

Telegy to set interrupt from MCDEM

Telegy to reset interrupt from MCDEM

Telegy from stop to set interrupt

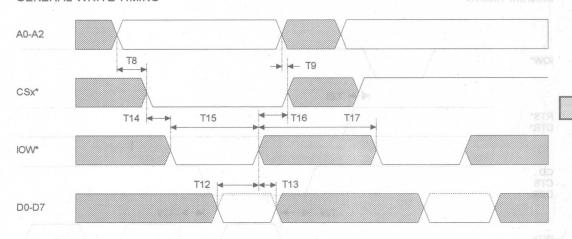
Telegy from IOR* to reset interrupt

Telegy from IOR* to reset interrupt

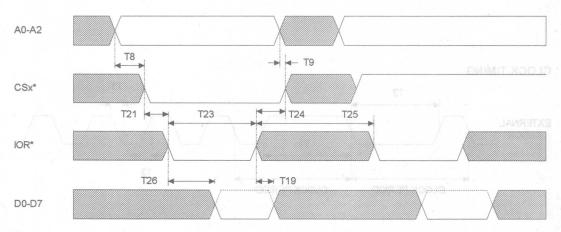
Telegy from IOW* to reset interrupt

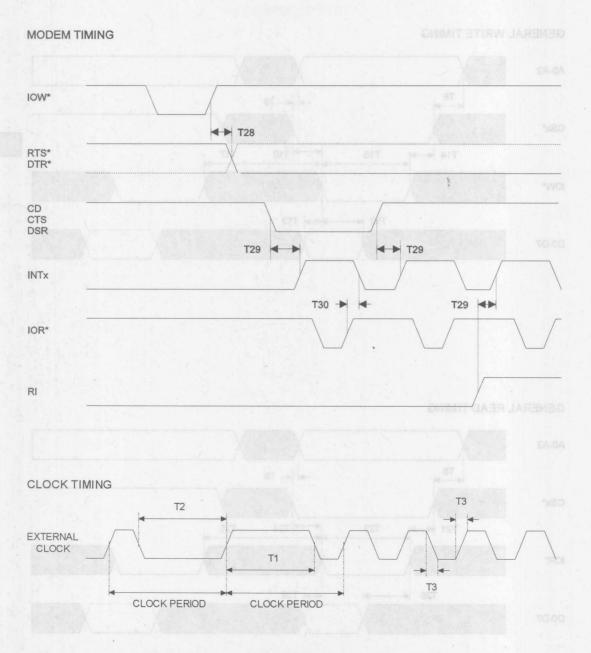
3

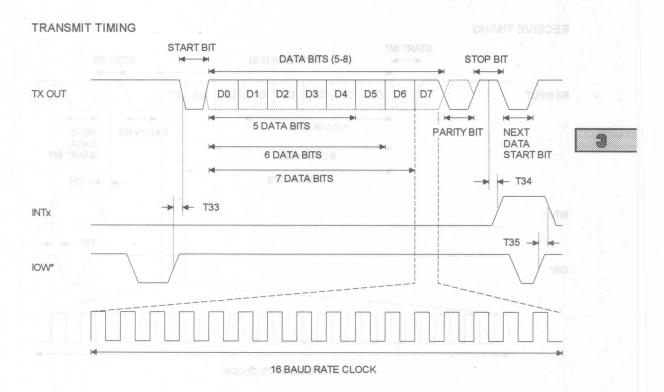


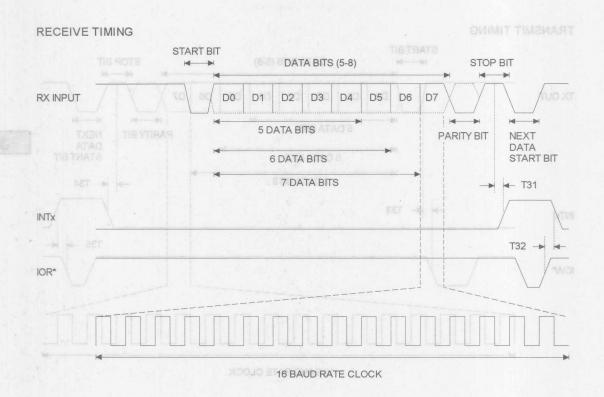


GENERAL READ TIMING









Printed September 6, 1994

QUAD ASYNCHRONOUS RECEIVER AND TRANSMITTER

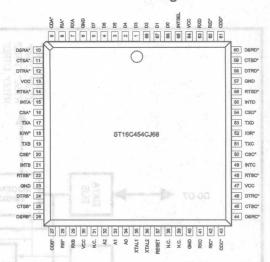
DESCRIPTION

The ST16C454 is a quad universal asynchronous receiver and transmitter. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C454 is an improved version of the NS16C450 UART with higher operating speed and lower access time. The ST16C454 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C454 provides internal loop-back capability for on board diagnostic testing.

The ST16C454 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

PLCC Package



FEATURES

- Quad ST16C450
- Pin-to-pin compatible to ST16C554
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

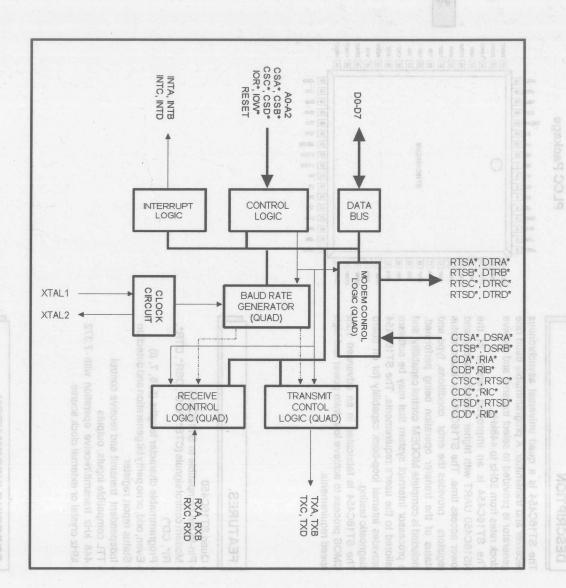
ORDERING INFORMATION

Part number ST16C454CJ68 ST16C454IJ68 Package PLCC PLCC Operating temperature 0° C to + 70° C

-40° C to + 85° C

3

BLOCK DIAGRAM



3-62

Symbol	Pin	Signal Type	Pin Description
the selected by		yoe soll Englisher Son Normal inter- grins pin to VCC	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
		alected when this	a si highio.
RX C-D	41,63	MCR bp-3 is set	Serial data input. The serial information (data) received from serial port to ST16C454 receive input circuit. A mark
Ms (LSR Bit-6).		ready (active to or-ed four trans ays low when at	(high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A-B	17.19		connection and connected to the 1x output internally.
TX C-D and all all all all all all all all all al	51,53	elect lito 2. To select line 1. To select line 1. To se	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or
			when the transmitter is disabled.
CS A-B*	16.20	elect line 0. To s	Address a
CS C-D*	50,54	l supput (active in	Chip select (active low). A low at this pin enables the ST16C454 / CPU data transfer operation. Each UART section of the ST16C454 can be accessed independently.
ATAL1me resemble reasonite in the modern	valle 25. Irans la detected. To indicate 1. Wrating a * 1.	y the interrupt of or, receiper data atus condition that a send. (active to ta ready to sent	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
	36	fliw nig Off fees	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	o firmedad edit 18	ave any effect of	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND	,	ninal ready. (ac	
GND		Lis raoy to no via the modern	Signal and power ground.
IOR*	TCI ed 52 lliws	f" auther MCR bit in be set to high	Read strobe (active low.) A low level on this pin transfers the contents of the ST16C454 data bus to the CPU.
ent the second of	riece88: oper high on this par	en the ownsmit of the control of the	Receive data ready (active low). This pin is the inverted output of internally "or-ed" four received data (LSR Bit-0) bits. Goes low when one of the UART's contains data in the

Symbol	Pin	Signal Type	Pin Description
DO is the least	rom the CPU	nal dati bus. Er formation to or bit of the data b	
		nput. The seri	output is selected when this pin is left open or connected to GND and MCR bit-3 is set to "1".
TXRDY G one	olgofa 39 , di) ec Idaaib al tugni	I port to ST16C4: gic one O d a sor back mode the K1 and connected	Transmit ready (active high). This pin is the output of internally "or-ed" four transmit empty signals (LSR Bit-6). This pin stays low when all four transmitters are empty.
		soutput. The serie	Address select line 2. To select internal registers.
	reset 88cal loc	onal start , stop a igh) sta l e during transmitter is dise	Address select line 1. To select internal registers.
A0 ent seldene nig INT A-B	34 aidt fa wol	I of (active low).	Address select line 0. To select internal registers. A 20
indeped-2 TAII coystal can be	elock input. A La plurto un TAL2 plurto un	the STOJOJS of external to this pin and Science Check the external check the external to the e	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
RTS C-D*motel	gen68,56 for a studied with the studied	out an Oaud rate out 2 or buffered	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive opera-
		ne (active low). A	
DTR A-B* DTR C-D*			
	46,58	I power ground.	Data terminal ready. (active low) To indicate that ST16C454 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0).
		its of the ST16C	Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have
		ata ready (active nternally "or-ed"	any effect on the transmit or receive operation.
		low when one of t	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and

Symbol	Symbol Pi		Pin Signal Type		Туре	Pin Description
0-tid		-Jid		E-fid	bit-4	the receiver input will be disabled during reset time.
CTS A-B* CTS C-D*	pn	rans holdl regis	11,25 45,59	modem I status interrupt	0	Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR A-B* DSR C-D*	VA O	Ini rong -tid	10,26 44,60	0	0	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive opera-
CD A-B* CD C-D*	rij	wor leng bit-	9,27 43,61	parity enable	eyen	Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modern.
RI A-B* RI C-D*	*5	RITA	8,28 42,62	INT enable	loop dack	Ring detect indicator. (active low) A low on this pin indicates the modern has received a ringing signal from telephone
VCC VCC		nevo erri	13,30 47,64	framing	veak lerrupt	line. 1983 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	9010	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	,
0	1	1	a LCR bit-7 is set to "1".	Line Control Register
1	0	0		Modem Control Register
1	0	1 1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

3

ST16C454 ACCESSIBLE REGISTERS

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
doi bete	M s e)	1 si la ad m it no		0 e low) Th t whose 4. CTS*	0 vilos) bu clion inpo MSR Bit	0 le of rest onition fun sading the	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0	1 solit	0	ISR Sent no wol	0 A (woler exchange	0 arty. (sotili ready to	0 in the sits 1 M3GO	0	0	int priority bit-1	int priority bit-0	int status
0	1 soil	1 oni ni	LCR	divisor latch enable	set break	set parity	even	parity enable	stop bits	word length bit-1	word length bit-0
1 solib	0	O iq sir	MCR	0 plevitos) in s beel	0 cindicator	0 hateb gnit	loop back	INT enable	Not used	RTS*	DTR*
1	0	1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1	1	1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C454 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2¹⁶-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

Not used except, in internal loop-back m:0-TIB RSI

0=disable the receiver ready interrupt. 1=enable the receiver ready interrupt.

IER BIT-1:

0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:

0=disable the receiver line status interrupt. Id seem 1=enable the receiver line status interrupt.

IER BIT-3:

0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 7-4: bns , stid pots, and its word length, stop bits, and its word length, stop bits,

All these bits are set to logic zero. Why we belos as

INTERRUPT STATUS REGISTER (ISR) WILLIAM BESTIT

The ST16C454 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C454 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

Р	D2	D1	D0	Source of the interrupt
1	1	1(8	0	LSR (Receiver Line Status Register)
2	1	0	10	RXRDY (Received Data Ready)
3	0	1	20	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	MSR (Modern Status Register)

1=a parity bit is generated during the tr:0-TIB RSI.

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

1=no interrupt pending.

ISR BIT 1-2:

Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:

These bits are not used and are set to "0".

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1011	6
1	0	on one of 7
1	100	8

LCR BIT-2:

The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	10
1	5	1-1/2
101	6,7,8	2

LCR BIT-3:

Parity or no parity can be selected via this bit. 0=no parity

1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4: SIME JOM BUTBOER ON THE TIME MAST

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.

0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for

1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5: and many "to of the ed lilly pall yights

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.

LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6: amag tid-blim ent to wol fills at XSI saft II Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).

0=normal operating condition.

1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7: THE STAR OLIAR STRAMMARDORS

The internal baud rate counter latch enable (DLEN). 0=normal operation.

1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:

0=force DTR* output to high. 1=force DTR* output to low.

The Interrupt Enable Ranister (IER) mas: 1-TIB ROM

0=force RTS* output to high. 1=force RTS* output to low.

MCR BIT-2:

Not used except, in internal loop-back mode.

BAUD RATE GENERATOR PRO:E-TIB ROM

0=set INT output pin to three state mode. 1=set INT output pin to normal operating mode.

MCR BIT-4:

0=normal operating mode.

1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and INT enable are connected to modem control inputs.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:

Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0: 0-7-0 2718 931

0=no data in receive holding register
1=data has been received and saved in the receive holding register. To BOTHS SOME

LSR BIT-1: |2 | r=8-2 aris 92

0=no overrun error (normal).

1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:

0=no parity error (normal).

1=parity error, received data does not have correct parity information.

LSR BIT-3:

0=no framing error (normal).

1=framing error received, received data did not have a valid stop bit. In

LSR BIT-4: Inemiliance aft at it show load-good

0=no break condition (normal).

1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5: memiliamon ant ai ti shom shadwa

0=transmit holding register is full. ST16C454 will not accept any data for transmission.

1=transmit holding register is empty. CPU can load the next character. The storm of the second of th

LSR BIT-6:

0=transmitter holding and shift registers are full. 1=transmitter holding and shift registers are empty.

LSR BIT-7:

Not used. Set to "0".

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:

Indicates that the CTS* input to the ST16C454 has changed state since the last time it was read.

MSR BIT-1:

Indicates that the DSR* input to the ST16C454 has changed state since the last time it was read.

MSR BIT-2

Indicates that the RI* input to the ST16C454 has changed from a low to a high state.

MSR BIT-3:

Indicates that the CD* input to the ST16C454 has changed state since the last time it was read.

3

MSR BIT-4:

This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:

This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6: "clume at taleiger galblod limenant=1

This bit is equivalent to MCR bit-2 during local loopback mode. It is the compliment of the RI* input.

MSR BIT-7: ratelogn fline bos gaibled restimenented

This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C454 provides a temporary data register to store 8 bits of information for variable use.

SIGNALS	RESET STATE
TX	High
OP1*	High and 197 si
OP2*	High and wol
RTS*	High
DTR*	High
INT	Three state
RxRdy*	High all ant soni
TxRdy	Low

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR		
50 1000	2304	=normal operal =enable loca		
75 ms 4) n	1536	ansmitter outp		
	80 1047			
	857			
150	768	ected to the re-		
	384			
600	192	.etuqi		
1200	96 99			
2400	48	ra fully operation		
3600	dal ed 32 diane	re also operati		
4800	bold 24	ow the lower (b)		
7200	ntheo 116 Contro	stead of the fo		
9600	12 alloun	upts are still co		
19.2K	6			
38.4K	3			
56K	2	2.77		
115.2K	et to zerp perma	for used. Are s		

ST16C454 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0 :0-TI8 #2
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	
MCR	MCR BITS 0-7=0 leight prible
LSR	LSR BITS 0-4=0,
	LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, 00000000000000000000000000000000000
MSR	BITS 4-7=input signals

AC ELECTRICAL CHARACTERISTICS

 $T_{\star}=0^{\circ}$ - 70° C, Vcc=5.0 V ± 1.0% unless otherwise specified.

Symbol	Parameter		Min	Limits Typ	Max	Units	Conditions
T ₁ T ₂ T ₃ T ₈ T ₉	Clock high pulse duration Clock low pulse duration		50 50	SOITSI	CTER	ns ns	External clock
T ₃	Clock rise/fall time	in a like	0000 00	wreitto s	10	ns	=0° - 70° C. Voc=5
T ₈	Chip select setup time	fieri.	15	Metalinin 8	esina a	ns	-g -10 C, VCC-3
T _o	Chip select hold time		0			ns	
Τ.,	Data set up time		15			ns	lodmys
T ₁₃	Data hold time	nik	15		Toled	ns	tomings
1 22	IOW* delay from chip select	1330	10			ns	
146	IOW* strobe width	8.0	50		le	ns	V Clock in
100	Chip select hold time from IOW*		0		lev		V Clocking
T ₁₇	Write cycle delay		55		100	ns	V. Input low
Tw	Write cycle=T ₁₅ +T ₁₇	2.9	105			ns	V input hig
T ₁₉	Data hold time		15	23110	ioo lis r	ns	V Output le
Tar	IOR* delay from chip select	B 3	10	, ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	THE PERSON	ns	V Output 1
22	IOR* strobe width		65		insmuo	ns	rog pvA
24	Chip select hold time from IOR*		0		111011110	ns	sel tugni oo'
T ₂₅	Read cycle delay		55			ns	L Clock let
11	Read cycle=T ₂₃ +T ₂₅		115			ns	10,
T ₂₆	Delay from IOR* to data				35	ns	100 pF load
T ₂ ,	Delay from IOW* to output				50	ns	100 pF load
T ₂₉	Delay to set interrupt from MODEN input	1			70	ns	100 pF load
T ₃₀	Delay to reset interrupt from IOR*				70	ns	100 pF load
1 24	Delay from stop to set interrupt				1 _{Rclk}	ns	100 pF load
32	Delay from IOR* to reset interrupt				200	ris	100 pF load
33	Delay from initial INT reset to trans start	mit	8		24	*	
T ₃₄	Delay from stop to interrupt				100	ns	
T ₃₅	Delay from IOW* to reset interrupt				175	ns	
144	Delay from stop to set RxRdy				1 _{RCLK}		A
T ₄₅	Delay from IOR* to reset RxRdy				1	μS	
46	Delay from IOW* to set TxRdy				195	ns	
T ₄₇	Delay from start to reset TxRdy				8	*	
N	Baud rate devisor		1		216-1		

Note 1: * = Baudout* cycle

3

ABSOLUTE MAXIMUM RATINGS

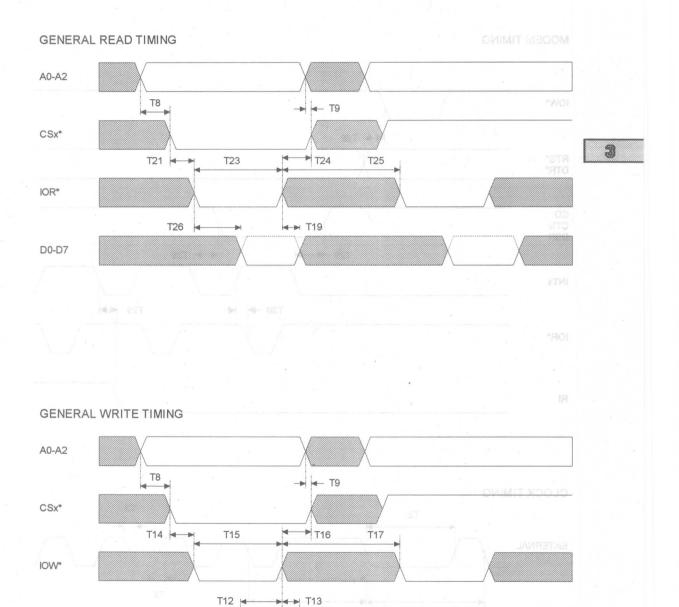
Supply range 7 Volts
Voltage at any pin
Operating temperature
Storage temperature
Package dissipation

7 Volts
GND-0.3 V to VCC+0.3 V
0° C to +70° C
-40° C to +150° C

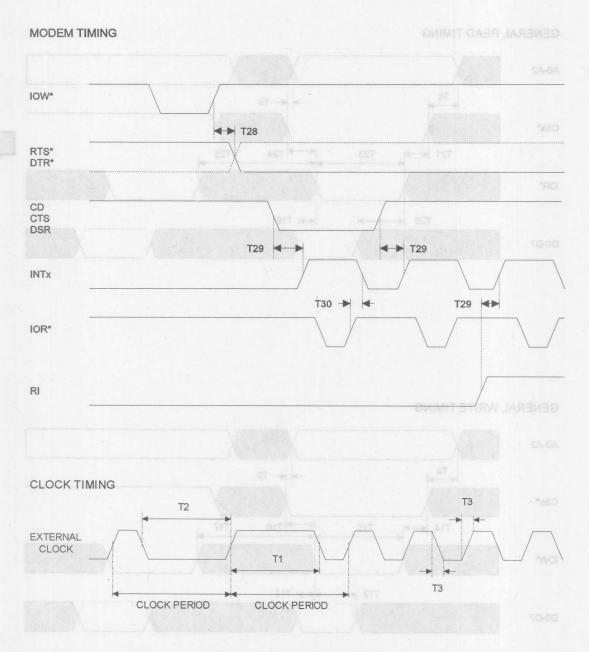
DC ELECTRICAL CHARACTERISTICS

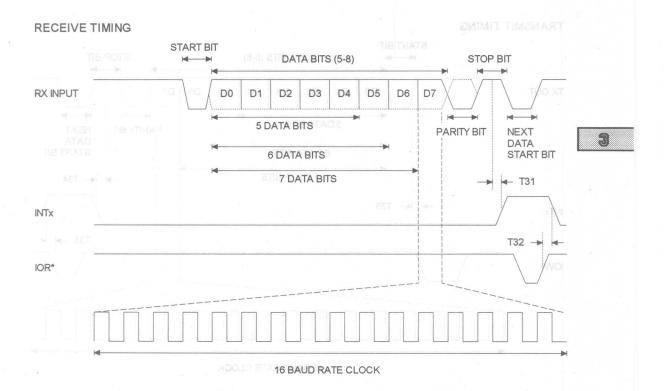
 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

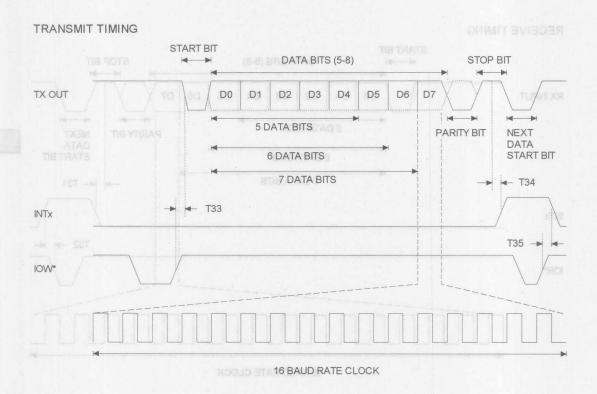
Symbol	V _{ILCK} V _{IHCK} V _{IHCK} V _{ILCK} Clock input low level Clock input high level Input low level Input high level Output low level on all outputs Output high level Avg power supply current Input leakage Clock leakage			nbol		Min	Limits Typ	Max	Units	Condition	ons
VILCK VIHCK VIH VOL VOH ICC IIL ICL				2.2	0.6 VCC 0.8 VCC 0.4 6 ±10 ±10	V V V V mA	I _{OL} = 6 mA I _{OH} = -6 mA				
bad	30.00t	SU	35	15			sisb r	t*901 m	Delay fre	T	
	100 pF l										
	100 pF li 100 pF li 100 pF l	ns ns ns							Delay to Delay fro		
		en en		. 8					siari		
							to reset set RxR		Delay fro		
								m IOR* I m IOW* m start to			
			216-4								



D0-D7



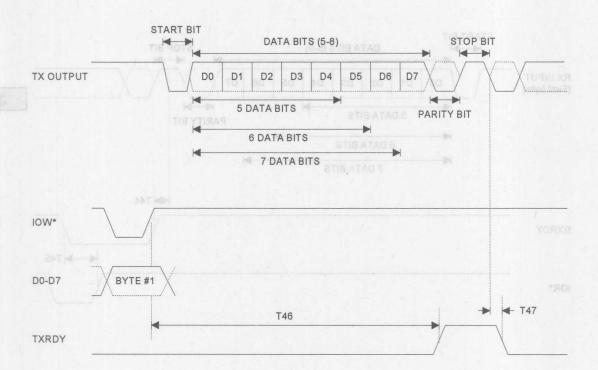




RXRDY TIMING

START BIT DATA BITS (5-8) STOP BIT RX INPUT D0 D1 D2 D3 D4 D5 D6 (First byte) 3 5 DATA BITS PARITY BIT 6 DATA BITS 7 DATA BITS **◆** T44 RXRDY IOR*

TXRDY TIMING



Printed September 6, 1994

QUAD ASYNCHRONOUS RECEIVER AND TRANSMITTER

DESCRIPTION

The ST68C454 is a quad universal asynchronous receiver and transmitter with modem control signals. Designed to interface with MOTOROLA, ROCKWELL, HITACHI bus and other popular microprocessors. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

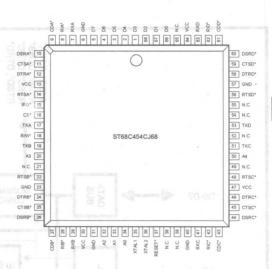
The ST68C454 is an improved, quad version of the NS16450 UART with faster operating access time. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. Complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

The ST68C454 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

FEATURES

- · Motorola, Rockwell, Hitachi bus compatible
- Quad ST16C450
- Modem control signals (CTS*,RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- · Status report register
- TTL compatible inputs, outputs
- 448 kHz transmit/receive operation with 7.372 MHz external clock source

PLCC Package



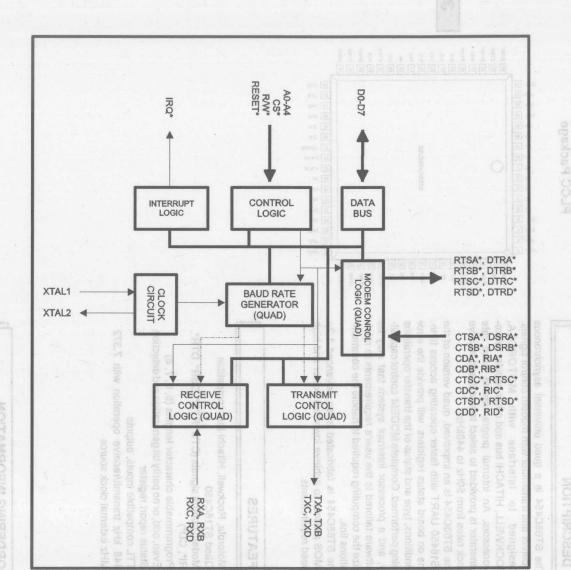
3

ORDERING INFORMATION

Part number ST68C454CJ68 ST68C454IJ68 Package PLCC PLCC Operating temperature 0° C to +70° C -40° C to +85° C

08-8

BLOCK DIAGRAM



3-80

Symbol	Pin	Signal Type	Pin Description
D7-D0	5-66	1/0	Bi-directional data I/O. Eight bit, three state data bus to
	(active tow). A lo	A-D indicator it modern has n re,	transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B	7,29		
RX C/D and fair		end A-11 (active a ready to send	Serial data input . The serial information received from MODEM or RS232 to ST68C454 receive circuit. A mark
) will set this pir be set to high.	ler (MOR bit-1 let this pur wit	(high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B	17,19 (wol	ovites) G-A br	
itions cd/2 XT effect on the	oroo 51,53v bu	airol fu 0 .tion in iding the MSR E output.	Serial data output A. The serial data of channel A is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS* 10 98 J) 8	low). This pin is but he 16 cential	emally toned" f	Chip select (active low). A low at this pin will enable the
	ie JakT's conta	wwhen one of thing register	UART A-D CPU data transfer operation.
	35 ni niq diriT. (n Kanpis Vigma kir	I ady (active hig	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal
	our transmitters	ys law when all t	internal circuit and baud rate generator for custom transmission rates.
XTAL2	AU mot saft to el 36 AU noct satt to el	1	Crystal input 2. See XTAL1.
R/W*	81 Nemal pogisters,	2. To select in	Read/Write strobe. A low on this pin will transfer the contents of the CPU data bus to the addressed register. A high on this pin will transfer the contents of the ST68C454
		t f. To select in	data bus to the CPU.
CD A/B*	9,27		
CD C/D*	.a.ə/a43,61sməfr	i 0. Tolselect in	Carrier detect A-D (active low). A low on this pin indicates that carrier has been detected by the modern.
GND g nig sin	6,23,31 40,57	put. (s O lve low	
		nabled by the inf	
	delia10,26 by tev		
DSR C/D*	44,60 noini	dem status cond	Data set ready A-D. (active low) A low on this pin indicates that MODEM is ready to exchange data with UART.

Symbol	Pin	Signal Type	Pin Description
RI A/B*	8,28	In data I/O. Eigh	7-D0 5-66 VO Bi-direction
RI C/D*edi zi 0	42,62	mailed to or fer it of the data bus or transmitted	Ring detect A-D indicator . (active low) A low on this pin indicates that modem has received a ringing signal from telephone line.
RTS A/B*	14,22		XA/8, 7.29
RTS C/D* /so mam A /luoni on grand on Ismetys mont	C454 receive	input. Ohe seri RS232 to ST68 contend a space of, mode the RX	Request to send A-D. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to low state. After the reset this pin will be set to high.
	11,25	and commented to	nolloennoo
top and parity during reset,	45,59 to atab lanes , hata lanoilibt uste (rigin) was limenant selt re	ria this pin with a will be held in a	Clear to send A-D. (active low) The CTS* signal s a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmitter output.
RXRDY*	38 ow at this pin a coperation.	O O O O O O O O O O O O O O O O O O O	Receive data ready (active low). This pin is the inverted output of internally "or-ed" four received data (LSR Bit-0) bits. Goes low when one of the UART's contains data in the receive holding register.
TXRDY and a	ed uso loolo	b his po and XT cuit. An external if and baud rate a	Transmit ready (active high). This pin is the output of internally "or-ed" four transmit empty signals (LSR Bit-6). This pin stays low when all four transmitters are empty.
A4	50	1	Address line 4. To select one of the four UARTS.
A3	20	d 2. See XTAL*	Address line 3. To select one of the four UARTS.
A2	32		Address line 2. To select internal registers.
A1	33	the CPU.	Address line 1. To select internal registers.
		ct A-D (hctive for has been detecte	Address line 0. To select internal registers.
IRQ*	15	bru O und.	Interrupt output. (active low open collector) This pin goes low (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter
		dy A-D. (active to N is ready to ex	empty or modem status condition flag is detected on UART A-D.

Symbol Pin Signal Type		Signal Type	Pin Description				
DTR A/B*	12,24	Interrupt Ena	0 0 1 Interrupt Status Register				
DTR C/D*	46,58 97	Line outrol Modern Conf	Data terminal ready A-D. (active low) To indicate that ST68C454 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset.				
RESET*	37		Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.				
VCC	13,30 47,64		Power supply input.				

SERIAL PORT SELECTION GUIDE

CS*	A4	А3	UART X		
1	Х	X	X		
0	0	0	UART A		
0	0	1.1	UART B		
0	1	0	UART C		
0	1	1	UART D		

will transfer the contents of the data bus (D7-D0) to the transmit holding register A-D whenever the trunsmitter holding register A-D or transmittershift register A-D or transmitter shift register A-D or sempty. The ignosmit holding register empty A-D has a will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A-D Note that a write operation should be performed when the transmit holding register empty flag is set. On the falling edge of the start bit, the receiver internal counter will start to count 7. 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX A-D is still low at the mid-bit sample of the start bit, vertying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX A-D input. Receiverstatus codes will be posted in the Line Staius Register A-D.

PROGRAMMABLE BAND RATE GENERATOR
The ST680454 contains a programmable Band Rate
Generator that is capable of taking any clock input
from DC-8 MHz and dividing it by any divisor from 1

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	19.94
0	oci 1st	two1 av	Data terminal ready A-D. (sot	Line Control Register
1	0		STSSC454 is ready to receive	Modem Control Register
111 515	0	rine1 Imi	Line Status Register	
est d'ann	1971	0	Modem Status Register	
er di 10	a Antib	110	Scratchpad Register	Scratchpad Register
0	0	0	register or after the reset.	LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER A-D

The serial transmitter section consists of a Transmit Hold Register A-D and Transmit Shift Register A-D. The status of the transmit hold register is provided in the Line Status Register A-D. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A-D whenever the transmitter holding register A-D or transmitter shift register A-D is empty. The transmit holding register empty A-D flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A-D. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX A-D is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX A-D input. Receiver status codes will be posted in the Line Status Register A-D.

PROGRAMMABLE BAUD RATE GENERATOR

The ST68C454 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2¹⁶-1. Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER A-D

The Interrupt Enable Register A-D masks the incoming interrupts from receiver ready, transmitter empty, line status and modern status registers to the IRQ* output pin.

IER BIT-0:

0=disable the receiver ready interrupt 1=enable the receiver ready interrupt

IER BIT-1:

0=disable transmitter empty interrupt 1=enable transmitter empty interrupt

IER BIT-2:

0=disable receiver line status interrupt 1=enable receiver line status interrupt

IER BIT-3:

0=disable the modem status register interrupt 1=enable the modem status register interrupt

IER BIT 7-4:

All these bits are set to logic zero.

INTERRUPT STATUS REGISTER A-D

The ST68C454 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A-D provides the source of the interrupt in prioritized manner. During the read cycle, the ST68C454 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

Р	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data
	15 10.	biba	dati	elve:	Ready) an agree palment
3	0	0	1	0	TXRDY(Transmitter
4	0	0	0	0	Holding Register Empty) MSR (Modem Status Register)

ISR BIT-0:

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine

1=no interrupt pending

ISR BIT 1-2:

Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:

These bits are not used and are set zero. Deau hold

LINE CONTROL REGISTER A-D

The Line Control Register is used to specify the asynchronous data communication format. The num-

ber of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:

These two bits specify the word length to be transmitted or received.

00=5 bits word length refriesce etsi bused lameths efficiency of the state of the s

LCR BIT-2:

The number of stop bits can be specified by this bit.

0=1 stop bit , when word length=5, 6, 7, 8 bits 1=1 and 1/2 stop bit , when word length=5 bits 1=2 stop bits, word length=6, 7, 8 bits 1=2 stop bits, word length=6, 7, 8 bits 1=3 stop bits

LCR BIT-3:

Parity or no parity can be selected via this bit. 0=no parity

1=a parity bit is generated during the transmission; receiver also checks for received parity

LCR BIT-4:

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.

0=odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.

1=an even parity bit is generated by calculating the number of even 1's in the transmitted data; receiver also checks for same format.

LCR BIT-5:s assured foundful shift flut , lenoterego

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.

LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

ber of the word length, slop bits, and pa: 6-118 LCR BIT-6:sq bits, and paid to be a slope bits.

Break control bit. In atshacrage philing ye before

1=forces the transmitter output (TX A-D) to go low to alert the communication terminal 0=normal operating condition

LCR BIT-7:

The internal baud rate counter latch enable (DLEN).
0=normal operation
1=select divisor latch register

MODEM CONTROL REGISTER A-D

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:

0=force DTR* output to high 1=force DTR* output to low brown as two slid gore 1=0

MCR BIT-1: and 8 , 7 ,8=ntonal brow and gots S=1

0=force RTS* output to high 1=force RTS* output to low

MCR BIT2-3:

x=not used and arth princip between a fild yilling a=1.

MCR BIT -4:

0=normal operating mode

1=enable local loop-back mode (diagnostics). The transmitter output (TX A-D) is set high (Mark condition), the Receiver inputs (RX A-D, CTS A-D*, DSR A-D*, CD A-D*, and RI A-D*) are disabled. Internally, the transmitter output is connected to the receiver input and DTR A-D*, RTS A-D* and MCR A-D bit2,3 are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IER A-D.

MCR BIT 5-7: vinso 1=4-TIS 90 1 bns 1=8-TIS 90 1

Not used. Are set to zero permanently.

LINE STATUS REGISTER A-D

This register provides the status of data transfer to CPU.

LSR BIT-0: ximoing level published provides A34 388T3 enT

0=no data in receive holding register

1=a data has been received and saved in the receive holding register

LSR BIT-1: needed of level formering teering and apply

0=no overrun error (normal)

1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:

0=no parity error (normal)

1=parity error, received data does not have correct parity information

LSR BIT-3: hotelpa 9 auf

0=no framing error (normal)

1=framing error received, received data did not have a valid stop bit

LSR BIT-4: A SOME SIZM

0=no break condition (normal)

1=receiver received a break signal (RX was low for one character time frame)

LSR BIT-5:

0=transmit holding register is full; ST68C454 will not accept any data for transmission

1=transmit holding register is empty; CPU can load the next character

LSR BIT-6:

0=transmitter holding and shift registers are full 1=transmitter holding and shift registers are empty

LSR BIT-7:

Not used, set to "0". and but beaution and alid seem?

MODEM STATUS REGISTER A-D

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:

Indicates that the CTS* input to the ST68C454 has changed state since the last time it was read.

MSR BIT-1:

Indicates that the DSR* input to the ST68C454 has changed state since the last time it was read.

MSR BIT-2:

Indicates that the RI* input to the ST68C454 has changed from a low to a high state.

MSR BIT-3:

Indicates that the CD* input to the ST68C454 has changed state since the last time it was read.

MSR BIT-4:

This bit is equivalent to RTS in the MCR. It is the compliment of the CTS* input.

MSR BIT-5:

This bit is equivalent to DTR in the MCR. It is the compliment of the DSR* input.

MSR BIT-6:

This bit is equivalent to MCR bit-2 during local loopback mode. It is the compliment of the RI* input.

MSR BIT-7:

This bit is equivalent to MCR bit-3 during local loopback mode. It is the compliment to the CD* input.

SCRATCHPAD REGISTER A-D

ST68C454 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

В	AUD RATE	16xCLOCK %ERROR	DVISOR
	50	2304	000
	75 150	1536 768	000
	300 600 1200 2400	384 192 96 48	100
0	4800 7200 9600 19.2	24 16 981 12 6	010
	38.4K	3 2 AOJ	2.77

ST68C454 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER A-D	BITS 0-7=0
ISR A-D	BIT-0=1, BIT-7=0
LCR A-D	BITS 0-7=0
MCR A-D	BITS 0-7=0
LSR A-D	BITS 0-4=0, BITS 5-6=1, BIT-7=0
MSR A-D	BITS 0-3=0, BITS 4-7= input signals

SIGNALS	RESET STATE
TX A-D RTS A-D*	High High
DTR A-D*	High
IRQ RXRDY*	Three state mode High
TXRDY	Low

3

ST68C454 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	300 800 1260 2460	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	ISR SI	0	72.0 9800 19.2	0	0 and 484	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0 MOITIQU	MCR	0 TERNAL	O MSK EX	0	loop back	Not used	Not used	RTS*	DTR*
1 0 1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	стѕ	delta CD*	delta RI*	delta DSR*	delta CTS*
111	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

DLL and DLM are accessible only when LCR bit-7 is set to "1".

AC ELECTRICAL CHARACTERISTICS

 T_A =0°-70° C, VCC=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
Т,	Clock high pulse duration	50			ns	
T,	Clock low pulse duration	50	TICS	Dictor	ns	External clock
T,	Clock rise/fall time		G-Dil	10	ns	O DWOIN LODGE
T ₁ T ₂ T ₃ T ₈ T ₉	Chip select setup time	5		la nanta	ns	00 700 0 1/00-5 0
T.	Chip select hold time	specified.	herwise	FO 550111	ns	3° - 70° C, Vcc=5.0
T.,	Data setup time	15			ns	
12	Data hold time from write or CS*	15		ret	ns	locine
T ₁₄	Write set up time	10		198	ns	10193
T ₁₅	Write strobe width	50			ns	
T,,	Chip select hold time from write	15			ns	V Clock incu
T ₁₇	Write cycle delay	45			ns	V Clock input
1 18	Data setup time	15			ns	V. Input low la
IW	Write cycle=T ₁₅ +T ₁₇	105			ns	rigin Jugal V
T ₂₄ 0 1	Data hold time	0			ns	Wolfingto V
25	Read cycle delay	25			ns	
Tr	Read cycle=T ₁₈ +T ₂₅	105			ns	V Oslput high
T ₂₇	Chip select pulse width	75			ns	ewon avA
T ₂₈	Delay from Write to output			50	ns	100 pF load
T ₂₉	Delay to set interrupt from MODEM input			35	ns eg	100 pF load
T ₃₁	Delay from stop to set interrupt			1 _{Rclk}	ns	100 pF load
T ₃₂	Delay from Read to reset interrupt			200	ns	100 pF load
T ₃₃	Delay from initial IRQ* reset to transmit start	8		24	* .	
T ₃₄	Delay from stop to interrupt		-	100	ns	
T ₃₅	Delay from Write to reset interrupt			75	ns	
Τ.,	Delay from stop to set RxRdy			1 _{RCLK}		
T,,	Delay from Read to reset RxRdy			1 1	μS	
T ₄₆	Delay from Write to set TxRdy			195	ns	6
T ₄₇	Delay from start to reset TxRdy			8	*	

^{* =} Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

Supply range Voltage at any pin Operating temperature Storage temperature Package dissipation GND-0.3 V to VCC+0.3 V 0° C to +70° C

-40° C to +150° C 500 mW

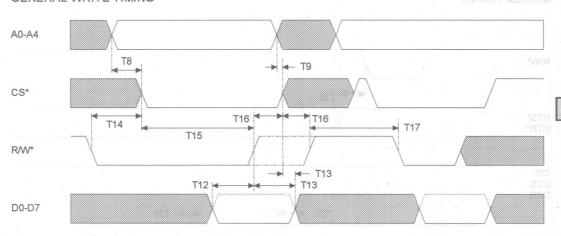
DC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ±10% unless otherwise specified.

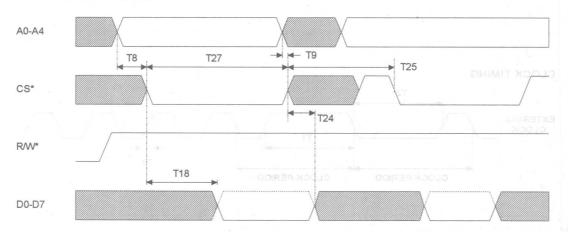
Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
VILCK	Clock input low level	-0.5	03/1	0.6	hol Vilma	Chip select
VIHCK	Clock input high level	3.0		VCC	V	Place ayore
VIL	Input low level	-0.5		0.8	V	guies sisci
VIH	Input high level	2.2		VCC	V	w - Vvnte oyota
V _{oL}	Output low level	25		0.4	Vem	I _{oL} = 6 mA on all outputs
V _{OH}	Output high level	2.4			V	I _{OH} = -6 mA
Icc	Avg. power supply current	c,	6	utput	mA	Delay from
I _{IL}	Input leakage Clock leakage		-MEGC	±10 ±10	μA μA	as Delay to se input

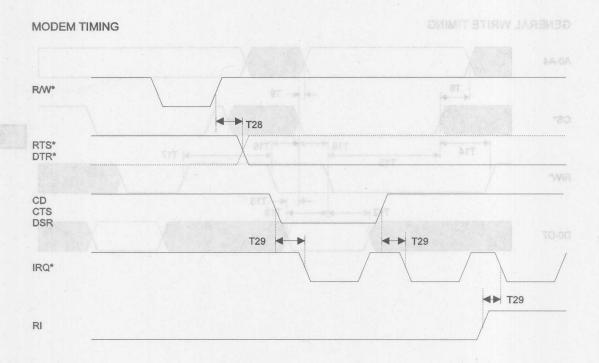
3

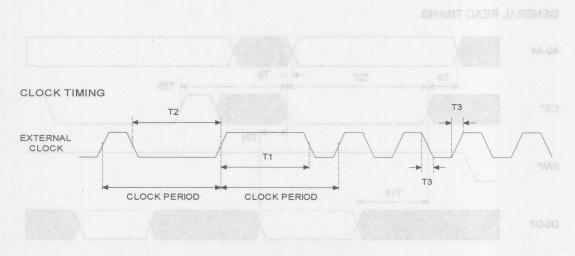


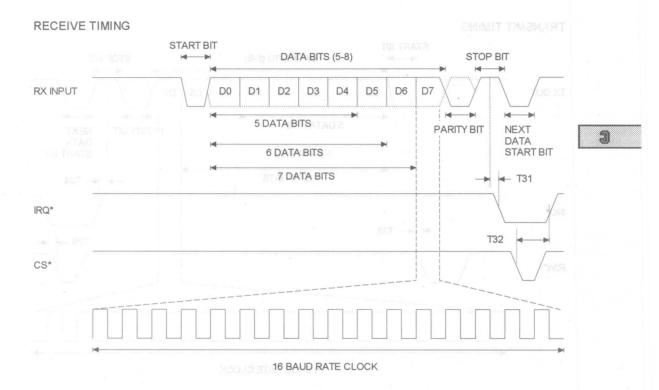


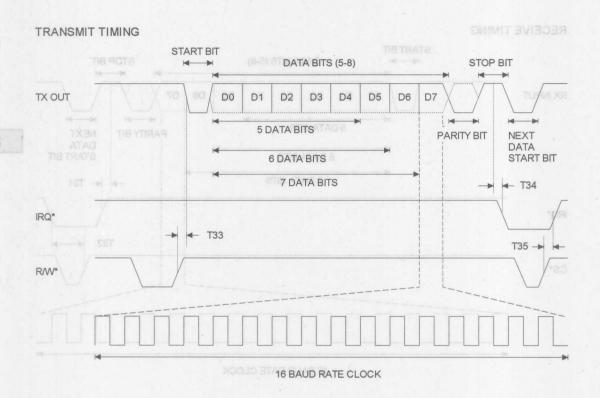
GENERAL READ TIMING



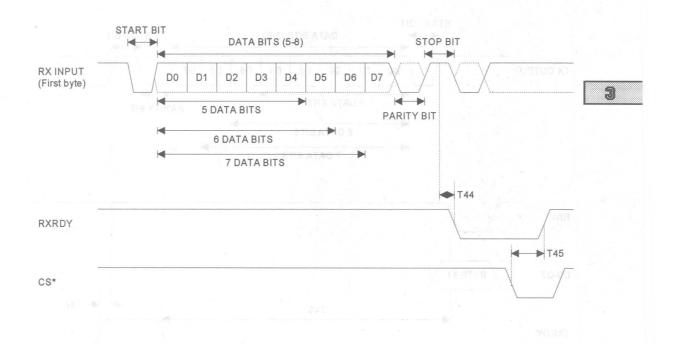




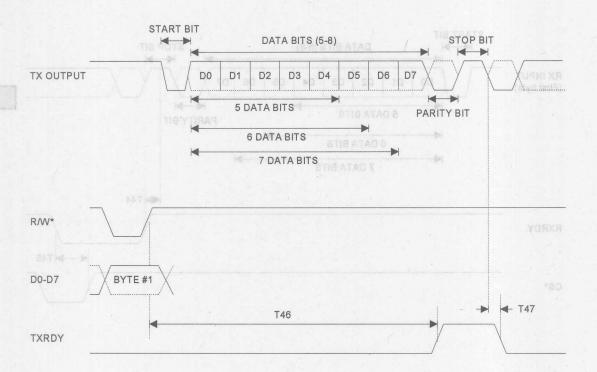




RXRDY TIMING



TXRDY TIMING





ST16C550

Printed September 6, 1994

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

DESCRIPTION

The ST16C550 is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C550 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C550 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C550 provides internal loop-back capability for on board diagnostic testing.

The ST16C550 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

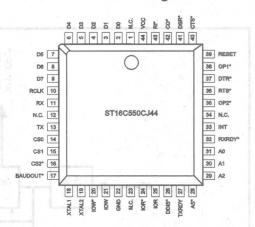
FEATURES

- Pin to pin and functional compatible to NS16550,VL16C550,WD16C550
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modern control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C450
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

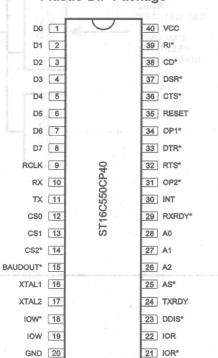
ORDERING INFORMATION

*Industrial operating range are available

PLCC Package



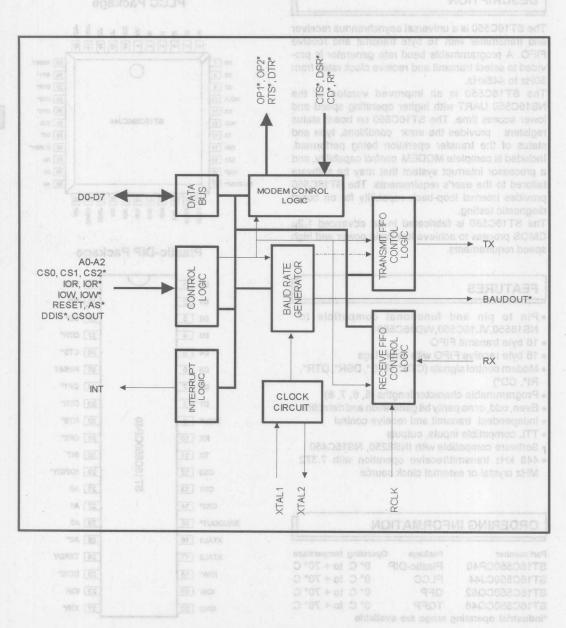
Plastic-DIP Package





UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOS

BLOCK DIAGRAM



Symbol	Pin	Signal Type	Pin Description
viii transfer the	nig slift no wol	sut 2 O\ pufferer pe (active low) 4 fulle CPU data t	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
	an active IOW* om IOFU to ST	ne. (active nigh) Note that only transfer deta f	Receive clock input. The external clock input to the ST16C550 receiver section if receiver data rate is different from transmitter data rate.
RX Zistensit Nige	10	I power ground. De. (active lew)	Serial data input. The serial information (data) received from serial port to ST16C550 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
XT out uses active or IOR input is to CPU during	11 Same as ICR* on active ICR* tom 5 T16C550	oe. (active high) Note that only	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS0	12	l (active low)	Chip select 1. (active high) A high at this pin enables the ST16C550 / CPU data transfer operation.
			Chip select 2. (active high) A high at this pin enables the
CS2*sidw.dglid s a besu ed n	h) Tel 4h in goes 2550 is full. 4 ca	eady. (I ctive hig IFO of the ST16 nulti-transfor.	Chip select 3. (active low) A low at this pin (while CS0=1 and CS1=1) will enable the ST16C550 / CPU data transfer operation.
			16x clock of the internal selected baud rate. RCLK pin is connected externally to BAUDOUT* pin to provide receive clock.
		elect line 1 To	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock

3

Symbol	Pin	Signal Type	Pin Description
	ght bil,71 ree st		Crystal input 2 or buffered clock output. See XTAL1.
	U90 eff met e and 81e fins e		Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
	i if receiver data	mitter data rate. a Input. The ser	Write strobe. (active high) Same as IOW*, but uses active high input. Note that only an active IOW* or IOW input is required to transfer data from CPU to ST16C550 during write operation. All the unused pin should be tied to VCC or GND.
GND	tuqni svisosi 03 colpol 20 ol) so	gas bronned	Signal and power ground.
IOR*/Ismetri	sidealb at tugni) ruqtuo (21 ad) of	sand calmacted	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C550 data bus to the CPU.
IOR ad lilw XT a	reset, local local	igh) state during ransmitter is dis	Read strobe. (active high) Same as IOR*, but uses active high input. Note that only an active IOR* or IOR input is required to transfer data from ST16C550 to CPU during read operation. All the unused pin should be tied to VCC or GND.
DDIS*		/ CPU deta tra O 1 2. (active high	Drive disable. (active low) This pin goes low when the CPU is reading data from the ST16C550 to disable the external transceiver or logic's.
	niq sidt 24 wol A 70 \ 08808878		Transmit ready. (active high) This pin goes high when the transmit FIFO of the ST16C550 is full. It can be used as a single or multi-transfer.
	greo sk 25 jugfuo len bued belbela k ol nig *TUOQU	of the internal s	Address strobe. (active low) A low on this pin will latch the state of the chip selects and addressed register (A2-A0). This input is used when signals are not stable for the duration of a read or write operation. If not required, tie the AS* input permanently low.
A2 and add exi	A humin soolo		
		ter basedons suc	Address select line 1. To select internal registers.

Symbol	Pin	Signal Type	Pin Description
A0 relicates 0A		ady, (alijva lov)	Address select line 0. To select internal registers.
RXRDY*	29	ready to exchi eve an Perract u	Receive ready. (active low) This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.
	y the modern	ect. (aQve low) bi an detected i	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
		a Leviscer and n	General purpose output. (active low) User defined output. See bit-3 modern control register (MCR bit-3).
RTS*	32	O Digital Video	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	33	0	Data terminal ready. (active low) To indicate that ST16C550 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
OP1*	34		General purpose output. (active low) User defined output. See bit-2 of modem control register (MCR bit-2).
RESET	Feditier	Interrupt En FIFD Contro Line Control Modern Con	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	riote no	l Scratchpad LSB of Divis MSB of Divi	Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.

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Symbol	Pin	Signal Type	Pin Description
	This pin gon	ited line 0. To set sady. (active low) PO is full. It can t	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
whenever a re-		utput, (active high y the interrupt ensure or receiver data to	Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modern.
RI*	39 39 Salasas (110) evi	atus condidos ilig	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC	40	T send. (active law)	Power supply input.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	A) olai	Receive Holding Register	Transmit Holding Register
0	0	1	and the second s	Interrupt Enable Register
0	: fliveniq	0	Interrupt Status Register	FIFO Control Register
1010	smiller	Thethan	outputs and internal registers.	Line Control Register
quit	0	0	the receiver input will be dise	Modem Control Register
1	0	1	Line Status Register	
ICIVI B	ai lyngb	0	Modem Status Register	
91191	d opp a	nollone)	Scratchpad Register	Scratchpad Register
0	0	0 0 0	reading the MSR BIT-4, CTS*	LSB of Divisor Latch
0	0	1	or receive operation.	MSB of Divisor Latch

ST16C550 ACCESSIBLE REGISTERS

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	IER	PIFO	SROTE FEERING LSR SIT	(8 1	ranguilte ig registe ismitter i io be cur	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0	1	0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0 0	efi v _o ma amelmi ja iloolo käi	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0	1	0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	(G ₀)	Dit o valid o the star siver from	int priority bit-2	int priority bit-1	int priority bit-0	int status
0	1	1 iges	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1	0	0	MCR	0	0 NGRAMM	0	loop back	OP2*	OP1*	RTS*	DTR*
1 01/4 NOC	0	1 yna ib vr	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	CD	RI	DSR	стѕ	delta CD*	delta RI*	delta DSR*	delta CTS*
1	1	1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

- A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.
- B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.
- C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C550 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

- A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.
- B) LSR BIT4-1 will specify which error(s) has occurred.
- C) LSR BIT-5 will indicate when the transmit FIFO is empty.
- D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.
- E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C550 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C550 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2¹⁶-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:

0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1: negw (witosmit dpin ac the ti

0=disable the transmitter empty interrupt. 1=enable the transmitter empty interrupt.

IER BIT-2:

0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:

0=disable the modern status register interrupt. 1=enable the modern status register interrupt.

IER BIT 7-4:

All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C550 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C550 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level man mow sid vitaging stid own sast

Р	D3	D2	D1	D0	Source of the interrupt
1	0	1	d 1 g	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0 beit	0	0 6d m	MSR (Modem Status Register)

*RECEIVE TIME-OUT:

This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be: $T = 4 \times 7$ (programmed word length) +12 = 40 bits Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:

T = 4 X 7(programmed word length) + 12 = 40 bits

Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

1=no interrupt pending. If note per political limited in

ISR BIT 1-3: In babeel of retoerand tent entirelies

Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7: sbom 024061 T8 ni al 022001 T8 nedW

These bits are not used and are set to zero in ST16C450 mode. BIT 6-7: are set to "1" in ST16C550 mode.

FIFO CONTROL REGISTER (FCR) so en sell religion

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:done or snotted for file of the end if

0=Disable the transmit and receive FIFO.

1=Enable the transmit and receive FIFO.

This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1: en onibled evideue emit dass no beviscar

0=No change. The subsyluo smit leads of

1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2: liw tup smilt .lid data and one ying on

0=No change. Alternal brown bernmannen W X a = T

1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3: + (rulphal brow barring googs X A = T

0=No change.

1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":

When ST16C550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":

When ST16C550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":

When ST16C550 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":

When ST16C550 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:

Not used.

FCR BIT 6-7: etal autota anil reviscon edu etdans=1

These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	1039 8UT 08 8 T9US
1	1	14
	native device!	

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Wo	rd lei	ngth	
0	0	CRXR	5	0	
0	1	Ready	6		
BIST BY	0	RXRD	7		
1	1 (time on	8		

LCR BIT-2:

The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	egist t t ais u
110	W "1" 05 les ens	1-1/2
1016	678	2

LCR BIT-3:

Parity or no parity can be selected via this bit.

0=no parity

1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4: saw if and Teel unit applies that a

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.

0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.

1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5: "Diff and in 3.19 of frelaviope of hid and I

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.

LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:

Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).

0=normal operating condition.

1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:

The internal baud rate counter latch enable (DLAB). 0=normal operation.

1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0: Office and halfqme at

0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1: half for all filled net

0=force RTS* output to high. 1=force RTS* output to low.

MCR BIT-2:

0=set OP1* output to high.
1=set OP1* output to low.

MCR BIT-3:

0=set OP2* output to high.
1=set OP2* output to low.

MCR BIT-4: shom ORIR ent of and gore bilev s

0=normal operating mode. 1843 943 144 484 845 100 224

1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:

Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:

0=no data in receive holding register or FIFO.

1=data has been received and saved in the receive

3

holding register or FIFO.

LSR BIT-1: His southern edit almineo nalaiger ain'i

0=no overrun error (normal).

1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:

0=no parity error (normal).

1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:

0=no framing error (normal).

1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4: And doing tea at (XT) broken refilmented

0=no break condition (normal).

1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5: mod method off denoterade gliul en

0=transmit holding register is full. ST16C550 will not accept any data for transmission.

1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:

0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In
FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:

0=Normal.

1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:

Indicates that the CTS* input to the ST16C550 has changed state since the last time it was read.

MSR BIT-1: Then bevieces not allosto oute revisor

Indicates that the DSR* input to the ST16C550 has changed state since the last time it was read.

MSR BIT-2: Indicates that the RI* input to the ST16C550 has changed from a low to a high state.

MSR BIT-3:

Indicates that the CD* input to the ST16C550 has changed state since the last time it was read.

MSR BIT-4:

This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5: also havisage bins bettimened with

This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:

This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:

This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C550 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RAT		x CLOCK DIVISOR	% ERROF
50		2304	
75		1536	
110		1047	0.026
134.5		857	0.058
150	Pg 001	768	2.00
300	l in the left	384	
600	Total levi	192	
1200	1 140 7	96	
2400		48	
3600	LUMBA	32	
4800		24	
7200		16	
9600		12	25
19.2K	t dioki	6	
38.4K		3	
56K	i sint.	2	2.77
115.2K		1811	1 .
	1		

ST16C550 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0,
	LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0,
	MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

RESET STATE
High amil quies 63
High amil blod at
High Welshald
High how edons "W
High old toels of
High reliab stayo chi
Low + Taglova sit
Low early block st

3

AC ELECTRICAL CHARACTERISTICS

 T_A =0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
T,	Clock high pulse duration	50	KSNOB (-A)		ns	UD RATE GENER
T ₂	Clock low pulse duration	50	SALTANIA SALAN	Service A	ns	External clock
T ₃ 118	Clock rise/fall time			10	ns	
T ₄	Baud out rise/fall time		8088	100	ns	100 pF load
T ₅	Address strobe width	30			ns	7
T.	Address setup time	30			ns	
T-	Address hold time	5			ns	50
T ₆ T ₇ T ₈ T ₉ T ₁₀	Chip select setup time	5			ns	av
T.	Chip select hold time	0	800.0		ns	110
T.o	CSOUT delay from chip select	10	880.0	25	ns	134.5
T ₁₁	IOR* to DDIS* delay			25	ns	100 pF load
T ₁₂	Data setup time	15			ns	Note: 1
T ₁₃	Data hold time	15		71	ns	Note: 1
T ₁₄	IOW* delay from chip select	10			ns	Note: 1
T ₁₅	IOW* strobe width	50			ns	2400
T ₁₆	Chip select hold time from IOW*	0			ns	Note: 1
T ₁₇	Write cycle delay	55			ns	4800
Tw	Write cycle=T ₁₅ +T ₁₇	105			ns	7200
T ₁₉	Data hold time	15		25	ns	0000
T ₂₁	IOR* delay from chip select	10			ns	Note: 1
T ₂₁ T ₂₃	IOR* strobe width	65			ns	38,4K
T ₂₄	Chip select hold time from IOR*	0	2.77		ns	Note: 1
T ₂₄ T ₂₅	Read cycle delay	55	1.5		ns	115.2K
Tr	Read cycle=T ₂₃ +T ₂₅	115			ns	
T ₂₆	Delay from IOR* to data			35	ns	100 pF load
T ₂₈ T ₂₉	Delay from IOW* to output			50	ns	100 pF load
T ₂₉	Delay to set interrupt from MODEM		1875	70	ns	100 pF load

3

AC ELECTRICAL CHARACTERISTICS

 $T_a=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

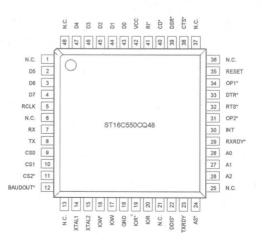
Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
T ₃₀	Delay to reset interrupt from IOR*			70	ns	100 pF load
T ₃₁ T ₃₂ T ₃₃	Delay from stop to set interrupt Delay from IOR* to reset interrupt Delay from initial INT reset to transmit	8	sewre it	1 _{RCIK} 200 24	ns *	100 pF load 100 pF load
T ₃₄	Delay from stop to interrupt Delay from IOW* to reset interrupt			100 175	ns ns	iodmy
T ₃₅ T ₄₄ T ₄₅ T ₄₆ T ₄₇	Delay from stop to set RxRdy Delay from IOR* to reset RxRdy Delay from IOW* to set TxRdy Delay from start to reset TxRdy	.0- .0-		1 _{RCLK} 1 195 8	μs ns *	V _{yok} Clack inpu V _{hex} Clack inpu V _{ppu} low I
Ν	Baud rate devisor	1	el	216-1	1	V., Input bight

Note 1: Applicable only when AS* is tied low
* = Baudout* cycle

52 Pin QFP Package

N.C. N.C. CTS* D5 2 38 RESET D6 3 37 OP1" D7 4 36 DTR* 5 35 RTS* RCLK N.C. 6 34 OP2* RX 7 ST16C550CQ52 33 INT TX 8 32 RXRDY CSO 9 31 A0 CS1 10 30 A1 CS2° 29 A2 BAUDOUT* 12 28 N.C. N.C. 13 27 N.C. 14 15 15 16 18 18 18 18 19 20 22 22 22 24 28 28 28 28 28 N.C. CTAL1 CTAL2 IOW' IOW OND N.C. IOR N.C. DDIS' XRDY

48 Pin TQFP Package



ST16C550

ABSOLUTE MAXIMUM RATINGS

Supply range
Voltage at any pin
Operating temperature
Storage temperature
Package dissipation

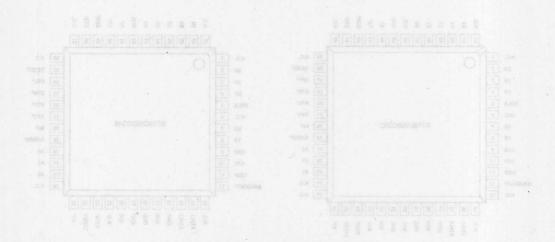
Supply range

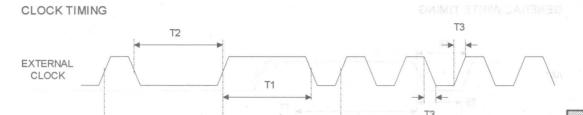
GND-0.3 V to VCC+0.3 V
OPERATOR OF C to +70° C
OPERATOR OF C TO +150° C
OPERATOR OF C T

DC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min Typ Max			Units	Conditio	ns
VILCK	Clock input low level	-0.5	Rdy	0.6	of Viol	Delay from	
VIHCK	Clock input high level	3.0	yb)	VCC	of VO	Delay from	
V.	Input low level	-0.5	vb5	0.8	LO ASIS	Delay from	
V _{IL} V _{IH}	Input high level	2.2		VCC	V		
Vol	Output low level on all outputs			0.4	V	I _{OL} = 6 mA	
V _{OL}	Output high level	2.4			V	I _{OH} = -6 mA	
Icc	Avg power supply current		6		mA		
I _{IL}	Input leakage		Wol bei	±10	μА	Applicable	
ICL	Clock leakage			±10	μА	" = Baudout	



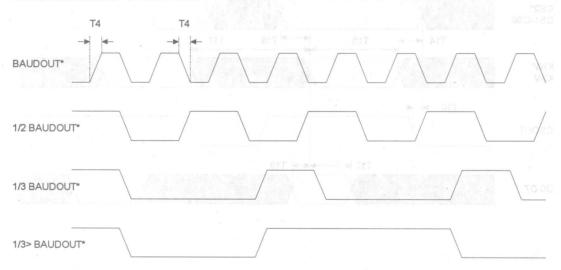


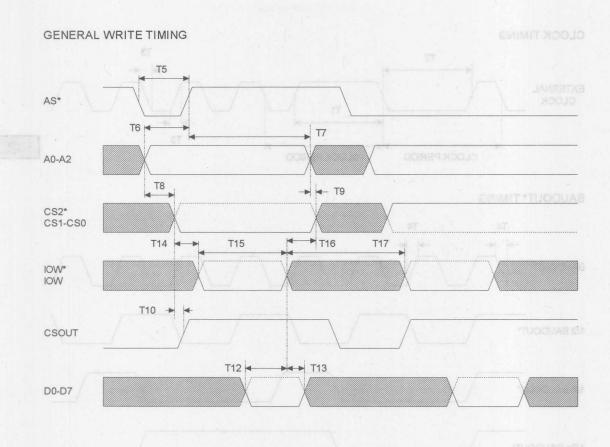
CLOCK PERIOD

3

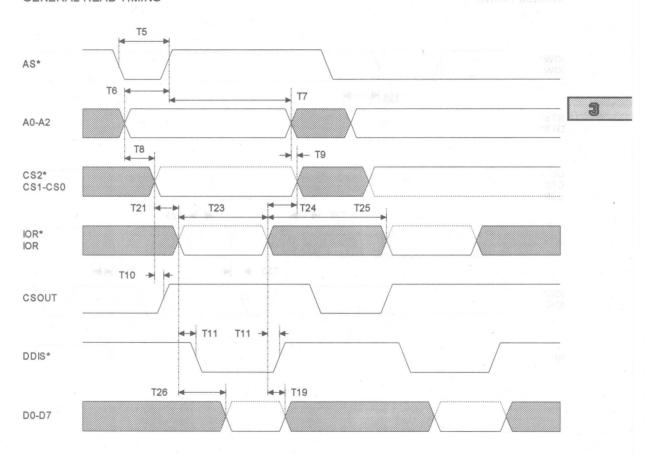
BAUDOUT* TIMING

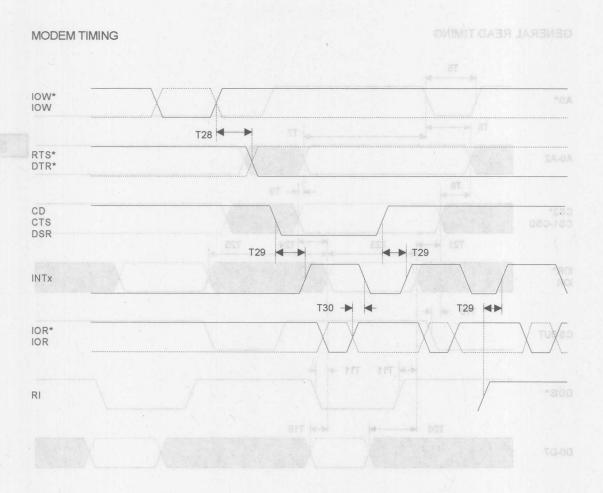
CLOCK PERIOD

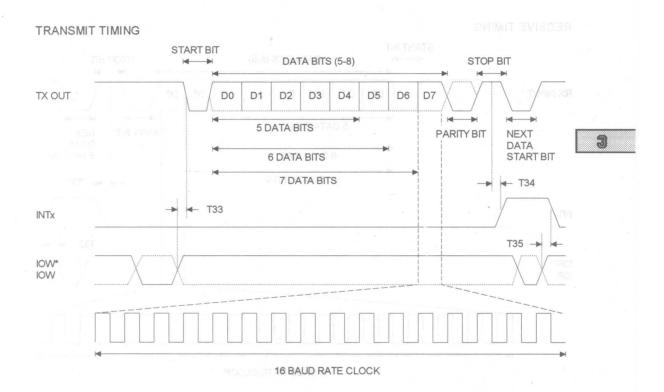


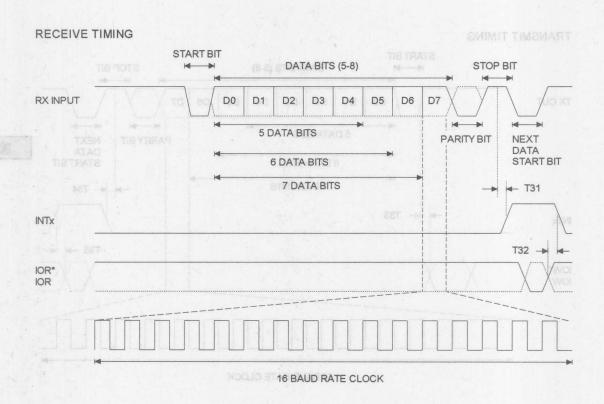


GENERAL READ TIMING

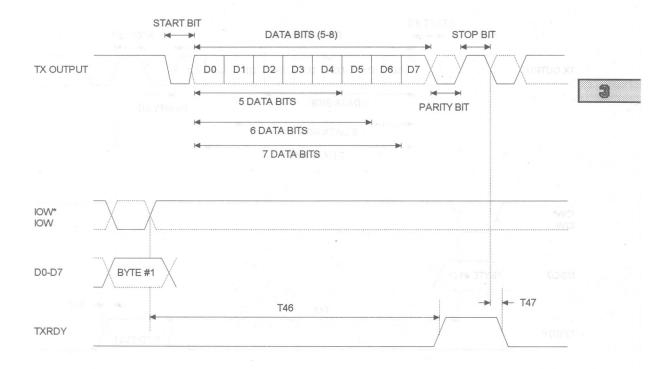






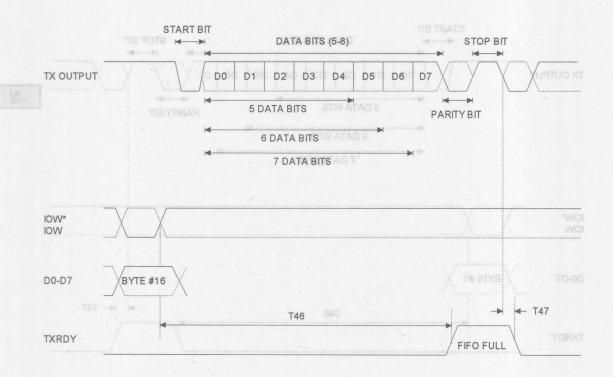


TXRDY TIMING FOR MODE "0"

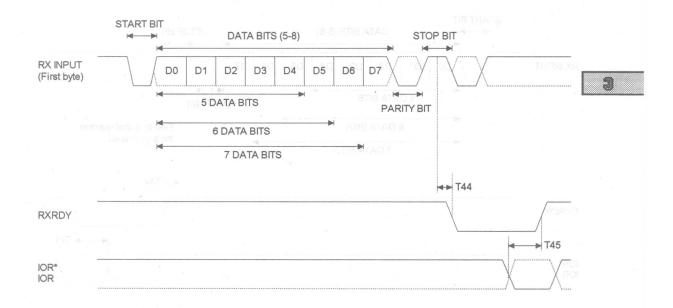


TXRDY TIMING FOR MODE "1"

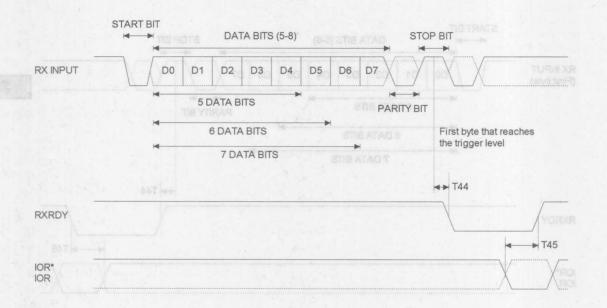
TXRDY TIMING FOR MODE "0"



RXRDY TIMING FOR MODE "0"



RXRDY TIMING FOR MODE "1"





Printed September 15, 1994

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

DESCRIPTION

The ST16C1550/51/52 is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C1550/51/52 is an improved version of the SSI 73M1550 and SSI 73M2550 UART with higher operating speed and lower access time. The ST16C1550/51/52 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C1550/51/52 provides internal loop-back capability for on board diagnostic testing.

The ST16C1550/51/52 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

FEATURES

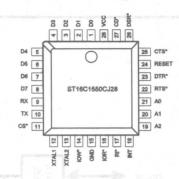
- Pin to pin and functional compatible to SSI 73M1550/2550
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modern control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Software compatible with INS8250, NS16C550
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

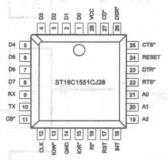
ORDERING INFORMATION

Part number	Package Op	erating	temperature
ST16C1550CP28	Plastic-DIP	0° C	to + 70° C
ST16C1550CJ28	PLCC	0° C	to + 70° C
ST16C1550CQ48	TQFP	0° C	to + 70° C
ST16C1551CP28	Plastic-Dip	0° C	to + 70° C
ST16C1551CJ28	PLCC	0° C	to + 70° C
ST16C1551CQ48	TQFP	0° C	to + 70° C
ST16C1552CQ52	QFP	0° C	to + 70° C
When also a Audia I are a second to a second		la la La	

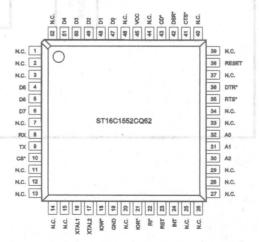
*Industrial operating range are available

PLCC Package

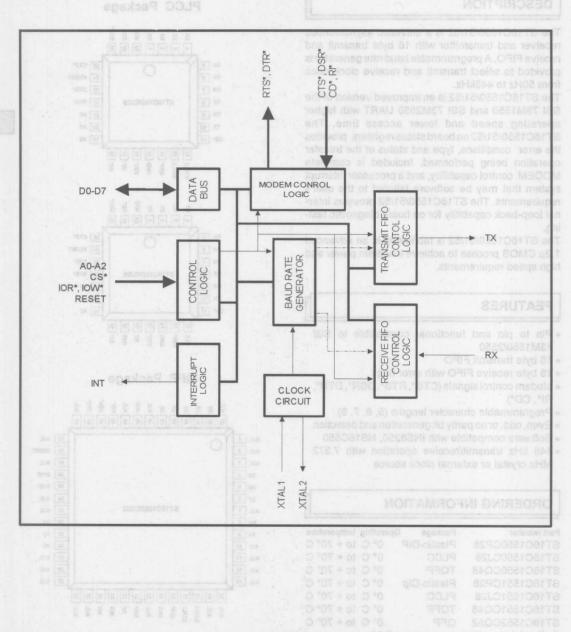




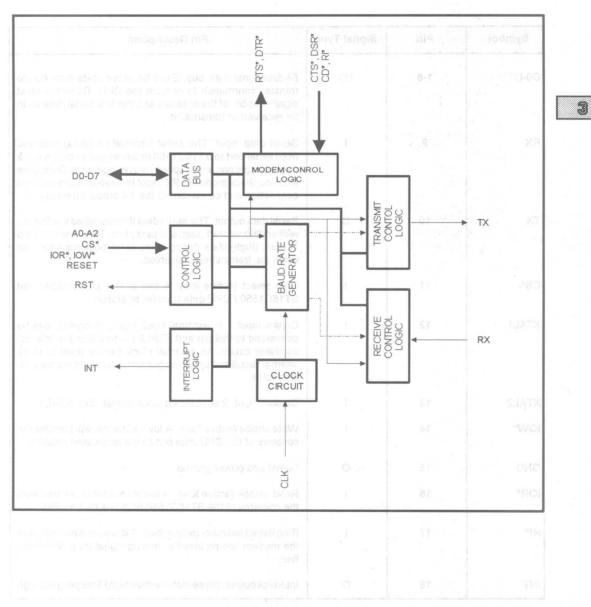
QFP Package



ST16C1550 BLOCK DIAGRAM



ST16C1551 BLOCK DIAGRAM



ST16C1550 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	1/0	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX	9	i de	Serial data input. The serial information (data) received from serial port to ST16C1550 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX X	10	0	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	11		Chip select (active low). A low at this pin enables the ST16C1550 / CPU data transfer operation.
XTAL1 X9 -	12		Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	13	1	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	14	- 1	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND	15	0	Signal and power ground.
IOR*	16	1	Read strobe (active low). A low level on this pin transfers the contents of the ST16C1550 data bus to the CPU
RI*	17	1	Ring detect indicator (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.
INT	18	0	Interrupt output. (three state / active high) This pin goes high

ST16C1550 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
talah misi da	em bir itres str tom the CPU-I ris red the rick s	nat data bus E formation to no bit of the data a dd or transmitted	(when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
A0-A2	21-19	1	Address select line. To select internal registers.
and (s) and (s	K input ir disabled to the TX ediput al feta istrenso d	nac edfi mojiosi	control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR* millions	percent and services of the se	igh) st.O. during ransmiller is gis at (active low) in / OFU detn in lock input / in ex	Data terminal read (active low). To indicate that ST16C1550 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have
	24	rquit, und band cot I pa (active tuwn)	Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	25 As no teveryou A	l bow i ground be (attive lov))	Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR bit-4. CTS* has no effect on the transmit or receive operation.
DSR*	er und etsb taar 26 Historiaa juucte magia phiguri	its of the ST140 I third pater (setty) In has received.	in the second of
CD*haved *GO		out (active high real output will or	The state of the s
VCC	28	1	Power supply input.
	Machydaigh, Ib	diput (unree at it	INT 18 O Intenupt of

ST16C1551 SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
samilter empty,	a available, tra flag is detected	bled b OVI e inten nor, receiver da status condition	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
AS at the transmil- in the modern to a low state, ote that this pin	e vindicate the vindicate vindicat	elect line. To sill p send (active lor ita ready to sen jister (MCR bit-t eset this pin will ave any effect o	Serial data input. The serial information (data) received from serial port to ST16C1551 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
XT Indicate that his pin can be	10 ive low). To	o ininst read (ac io is ready to r via the modern	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS* of Juquo 7	0 will st the DT state after writ	1" at the MCR bit ill be set to high	Chip select (active low). A low at this pin enables the ST16C1551 / CPU data transfer operation.
CLK not	or recr 21 e opera A high on this pin	on the Iransmit et (active high).	External clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
low*sime *WOI	grinut 13 aldsai	d internal registerer input will be d	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND seed on	se con 11 ions or	end (active low) action Out who a MSR bit-s. CT	Signal and power ground.
IOR*	15	operatibn.	Read strobe (active low). A low level on this pin transfers the contents of the ST16C1551 data bus to the CPU
DART, THE IN	niw 160 agns	ady (active low) s ready he exch ave any effect o	Ring detect indicator (active low). A low on this pin indicates
RST election of		tect (acove low) s been detected	Reset output (active high). The ST16C1551 provides a buffered reset output which is gated internally with MCR bit-2.
INT	18	aply Input.	Interrupt output. (three state / active high) This pin goes high

ST16C1550/51/52

ST16C1550 ST16C1551/1552

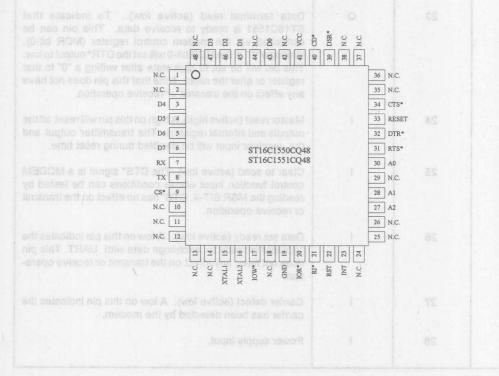
ST16C1551 SYMBOL DESCRIPTION

			AZ A1 A0 L READ MODE
Symbol	Pin	Signal Type	Pin Description
	Regist	FIFO Contro Line Contro Modern Cor	(when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
A0-A2		Solatchpad LSB of Divi	Address select line. To select internal registers.
RTS*		old 10 8 0 M	Request to send (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*	23		Data terminal read (active low). To indicate that ST16C1551 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
RESET	24		Master reset (active high). A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*	25		Clear to send (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR*	26	28 28 28 28	Data set ready (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD*	27	1 .	Carrier detect (active low). A low on this pin indicates the carrier has been detected by the modern.
VCC	28	- 1	Power supply input.

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PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	he1sine	enaldaria	(when enabled by the interrupt	Line Control Register
me1ett	0	0	e etab reviener name reviener	Modem Control Register
1	0	niel1ar o	Line Status Register	
1	1	0	Modem Status Register	
1	rectation	sm1tni	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	soithi o'	Penuest to send (active low).	MSB of Divisor Latch



ST16C1550 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	9 bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	LISIER 99 JULIA PIDET SUIS JOUTH	ede o rec nus en lot st	om o 0	0/ special mode	0 0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR III	RCVR trigger (MSB)	RCVR trigger (LSB)	0 / TX trigger (MSB)	0 / TX trigger (LSB)	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR ISR	0/ FIFOs enabled	0/ FIFOs enabled	0/ RXRDY	0/ TXRDY	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity	stop	word length bit-1	word length bit-0
1 0 0	MCR	0/power down	0 (01	0	loop back	INT enable	SOFT	RTS*	DTR*
1 0 1	LSR	0 / FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	стѕЯ	delta CD*	delta	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	- DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

DLL and DLM are accessible only when LCR bit-7 is set to "1".

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ST16C1551 ACCESSIBLE REGISTERS

A2 A1 A	0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0)	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	g bit-1	bit-0
0 0 0)	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
	pn	ric IER viec blort ent tiger aute trume	ster or re atus strupt s		0 / special mode	0 0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	980	FCR OFF	RCVR trigger (MSB)	RCVR trigger (LSB)	0/TX trigger (MSB)	0/TX trigger (LSB)	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0		ISR ini	0 / FIFOs enabled	0 / FIFOs enabled	0/ RXRDY	0/ TXRDY	int priority bit-2	int priority bit-1	int priority bit-0	int
0 1 1	0,4	LCR qoi	divisor latch enable	set break	set parity	even parity	parity	stop	word length bit-1	word length bit-0
1 0 0) -	MCR	0/power down	opp 0 qoo	0 0	loop back	INT enable	SOFT	RTS*	DTR*
1 ₀ 0 ₁ 1		LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity a error	overrun error	receive data ready
1 1 0	0 8	MSR	CD	RIST	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1		SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0)	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	1 0	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

- A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.
- B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.
- C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C1550/51/52 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

- A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.
- B) LSR BIT4-1 will specify which error(s) has occurred company register regions and illegabed
- C) LSR BIT-5 will indicate when the transmit FIFO is empty.
- D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.
- E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C1550/51/52 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C1550/51/52 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 216 -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty. line status and modem status registers to the INT output pin.

ST16C1551/1552

FIFO POLLED MODE OPERATION :0-TIR SI

0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1: and bus revision and ponis moustedo

0=disable the transmitter empty interrupt.

IER BIT-2:

0=disable the receiver line status interrupt. 1=enable the receiver line status interrupt.

IER BIT-3; one noinw vijoegz Illw 1-ATI8 78.1 (8

0=disable the modern status register interrupt.

1=enable the modern status register interrupt.

IER BIT 4:

This bit is not used and set to zero.

IER BIT 5:

0=disable the ISR bits 4-5 and MCR bit-7. 1=enable the ISR bits 4-5 and MCR bit-7 function.

IER BIT 6-7:

These bits are not used and set to zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C1550/51/52 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C1550/51/52 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level GLOHEWEDER GMATIMEMART

Р	D3	D2	D1	D0	Source of the interrupt
1	0	1	nithin ler (L	0	LSR (Receiver Line Status Register)
2	0	14	0	0	RXRDY (Received Data
	/ 19	egis	gnii	ilorio	Ready)
2*	e1 s	10	0	0	RXRDY (Received Data
	g re	niblo	f time	trans	time out) a resign file
3	0	0	110	0	TXRDY(Transmitter
	fima	isu	the .	of be	Holding Register Empty)
4	0	0	0	0	MSR (Modem Status
	Inm	tela	991	pallolo	Register)

*RECEIVE TIME-OUT: Impos of hale like refuseo

This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be: $T = 4 \times 7$ (programmed word length) +12 = 40 bits Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be: $T = 4 \times 7$ (programmed word length) + 12 = 40 bits Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

1=no interrupt pending.

ISR BIT 1-2:

Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3: Attack to puer for adoptional and recess

This bit is used with conjunction of ISR bit 0-2: 0=normal interrupt mode
1=receive time-out indicator when priority level is set to "2" (D0=0, D1=0, and D2=1)

ISR bit-4: ... a range of the last complete and all to

This bit is the compliment of TXRDY* (ST16C550) pin when IER bit-4 is set to "1".

0=transmitter is full

1=transmitter is empty or less than full

ISR bit-5:

This bit is the compliment of RXRDY* (ST16C550) pin when IER biot-4 is set to "1".

0=receiver is empty.

1=receiver is not empty

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:

0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:

0=No change.

1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:

0=No change, sort and loss of basis are still asort

1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:

0=No change.

1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":

When ST16C550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":

When ST16C550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":

When ST16C550 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":

When ST16C550 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:

These bits are used to set the transmit trigger levels. See receive FIFO trigger table.

3

FCR BIT 6-7:

These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	change 10
0.0	Y pirts from	TRXT bins Y04 XR esons
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

When ST16C550 is in ST16C450 mode:0-1TIB ROJ

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
ovito 1 sni)	ngir O mo	operation 2n mode "I 16C550 is 1.6 - IFO mode ne TXRDY 7 oin will bed ransmit FI 8 is complu

When ST16C550 is in FIFO mode (FCR :ST3 ROLL)

The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1 :8-
ger L ive	t the tractanit trig	a of 1-1/2 sha
1	6,7,8	e FIFS trigger

LCR BIT-3:

Parity or no parity can be selected via this bit. Jpo.J 0=no parity

1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.

0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.

1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format. To promise a affirm and a limit of the same format.

LCR BIT-5:

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.

LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:

Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).

0=normal operating condition.

1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:

The internal baud rate counter latch enable (DLEN). 0=normal operation.

1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

1=Clears the contents of the receive Fit:0-TIB ROM

0=force DTR* output to high. 0 of algol asinuso ali

MCR BIT-1: Ibsignonen al roumgtal aidsig MECOM

0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2: randgmen a applyong \$2\ha\033 r 08 r TS

0=normal operation of modernoons to said a secretary

1=software reset, set RST output to high.

MCR BIT-3:

0=set INT output pin to three state mode.
1=set INT output pin to normal operation mode.

MCR BIT-4:

0=normal operating mode.

1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, SOFT reset and INT enable are connected to modem control inputs.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-6:

Not used. Are set to zero permanently.

MCR bit-7:

0=normal mode.

1=power down mode. CLK, XTAL1, XTAL2, and baud rate generators are disabled.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:

0=no data in receive holding register or FIFO. 1=data has been received and saved in the receive holding register or FIFO. MOBR RUTATE MEGOM

LSR BIT-1: elists inemub ant septivoral status sidi-

0=no overrun error (normal), mebom sni mort send

1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:

0=no parity error (normal).

1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:61T2 edit of logn. 19 and tool estacion.

0=no framing error (normal).vol a mont because of

1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:

0=no break condition (normal).

1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:

0=transmit holding register is full. ST16C1550/51/52 will not accept any data for transmission.

1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:administration of the second secon

0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In
FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7: amilgroop sitt sittli abom Naad-goot Igoot

0=Normal

1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

3

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0: 100 for all 1 lad not have been all relations

Indicates that the CTS* input to the ST16C1550/51/52 has changed state since the last time it was read.

MSR BIT-1:

Indicates that the DSR* input to the ST16C1550/51/52 has changed state since the last time it was read.

MSR BIT-2:

Indicates that the RI* input to the ST16C1550/51/52 has changed from a low to a high state.

MSR BIT-3: abom 'ORIR and pl did gote bilev a

Indicates that the CD* input to the ST16C1550/51/52 has changed state since the last time it was read.

MSR BIT-4:

This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:

This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:

This bit is equivalent to SOFT reset in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7: reteiger filde timenen bas OFIF retilm

This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a

MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C1550/51/52 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	- yy
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

SIGNALS	RESET STATE
TX	High
SOFTreset	High
RTS*	High
DTR*	High
INT	Three state

3

ST16C1550/51/52 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0,
	LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0,
	MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

AC ELECTRICAL CHARACTERISTICS

 $T_{\Delta}=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
Т	Clock high pulse duration	50			ns	08
T	Clock low pulse duration	50	0.026		ns	External clock
T.	Clock rise/fall time	00	880.0	10	ns	External older
T ₁ T ₂ T ₃ T ₈ T ₉ T ₁₂	Chip select setup time	5	000.0		ns	150
T.	Chip select hold time	0			ns	300
T ₄₀	Data set up time	15			ns	008
T ₁₃	Data hold time	15			ns	1200
T ₁₄	IOW*delay from chip select	10			ns	2400
T ₁₅	IOW* strobe width	50			ns	3800
T ₁₆	Chip select hold time from IOW*	0		1	ns	4800
T ₁₇	Write cycle delay	55			ns	7200
Tw	Write cycle=T ₁₅ +T ₁₇	105			ns	0088
T ₁₉	Data hold time	15			ns	19.2K
T ₂₁	IOR* delay from chip select	10			ns	38.4K
T ₂₃	IOR* strobe width	65	2.77	1	ns	58K
24	Chip select hold time from IOR*	0		- 1	ns	115.2K
25	Read cycle delay	55		1	ns	
Tr	Read cycle=T ₂₃ +T ₂₅	115			ns	
T ₂₆	Delay from IOR* to data			35	ns	100 pF load
28	Delay from IOW* to output			50	ns	100 pF load
T ₂₉	Delay to set interrupt from MODEM input		COND	70	ns	100 pF load
T ₃₀	Delay to reset interrupt from IOR*			70	ns	100 pF load
31	Delay from stop to set interrupt			1 _{Rok}	ns	100 pF load
T ₃₂	Delay from IOR* to reset interrupt			200	ns	100 pF load
T ₃₃	Delay from initial INT reset to transmit start	8		24	. BITS 0-1	IER I IER
T ₃₄	Delay from stop to interrupt		rs 1-7=0	100	ns	ISR ISR
T ₃₅	Delay from IOW* to reset interrupt			175	ns 8	LCR LC

Note 1: * = Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

Supply range Voltage at any pin Operating temperature Storage temperature Package dissipation 7 Volts GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

DC ELECTRICAL CHARACTERISTICS

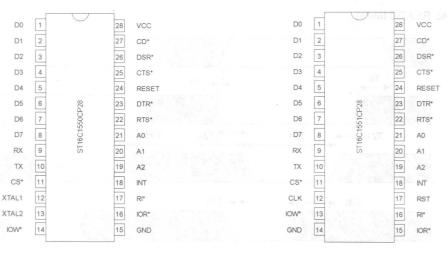
 $T_*=0^{\circ} - 70^{\circ}$ C, $Vcc=5.0 \text{ V} \pm 10\%$ unless otherwise specified.

3

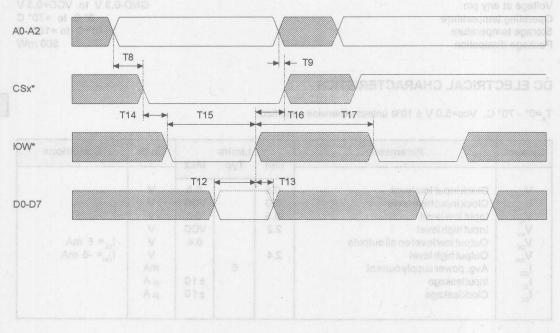
Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
VILCK VIHCK VIL VOL VOH ICC IIL ICC IL ICL	Clock input low level Clock input high level Input low level Input high level Output low level on all outputs Output high level Avg. power supply current Input leakage Clock leakage	-0.5 3.0 -0.5 2.2 2.4	6	0.6 VCC 0.8 VCC 0.4 ±10 ±10	V V V V MA μ A	I _{OL} = 6 mA I _{OH} = -6 mA

28 PIN PLASTIC-DIP ST16C1550

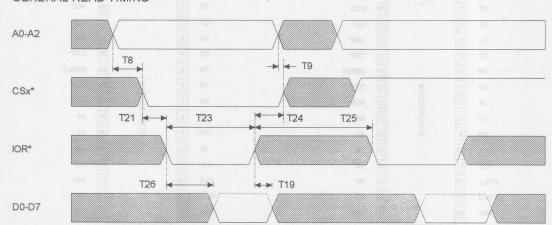
28 PIN PLASTIC-DIP ST16C1551



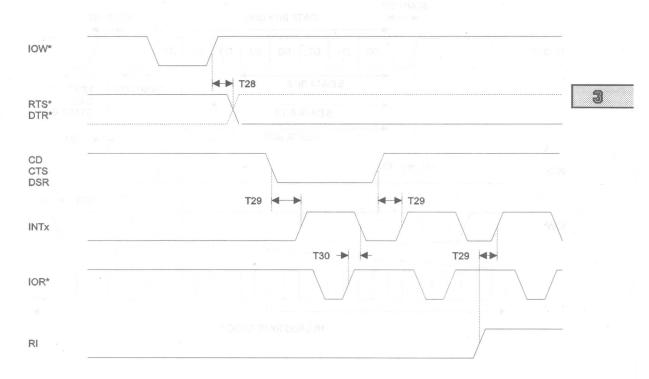


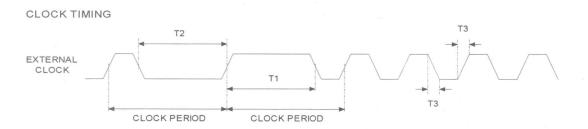


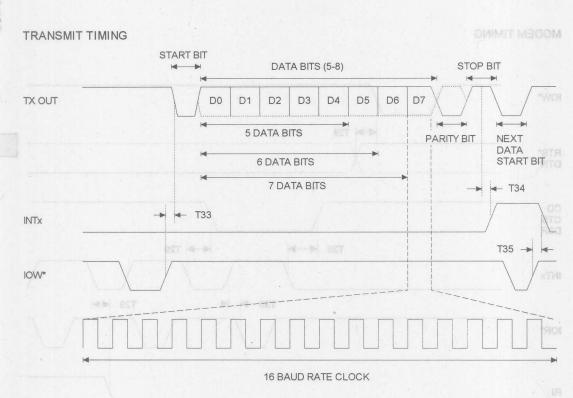
GENERAL READ TIMING

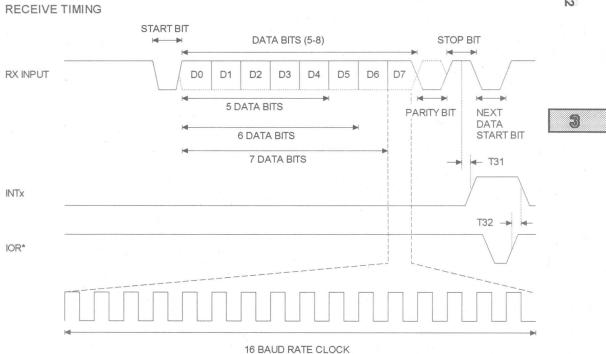


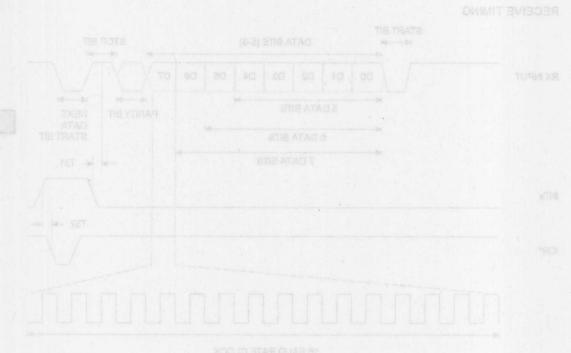
MODEM TIMING













ST16C2550

Printed September 7, 1994

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

DESCRIPTION

The ST16C2550 is a dual asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50Hz to 448kHz for each UART.

The ST16C2550 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C2550 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C2550 provides internal loop-back capability for on board diagnostic testing.

The ST16C2550 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

FEATURES

- Pin to pin and functional compatible to ST16C2450
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, -RI*. CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C550
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

ORDERING INFORMATION

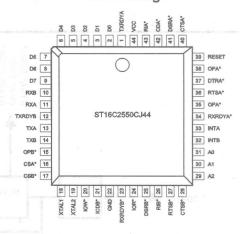
 Part number
 Package
 Operating temperature

 ST16C2550CP40
 Plastic-DIP
 0° C to + 70° C

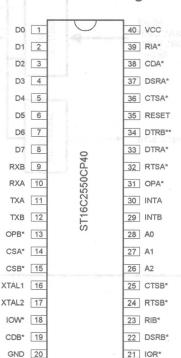
 ST16C2550CJ44
 PLCC
 0° C to + 70° C

*Industrial operating range are available

PLCC Package

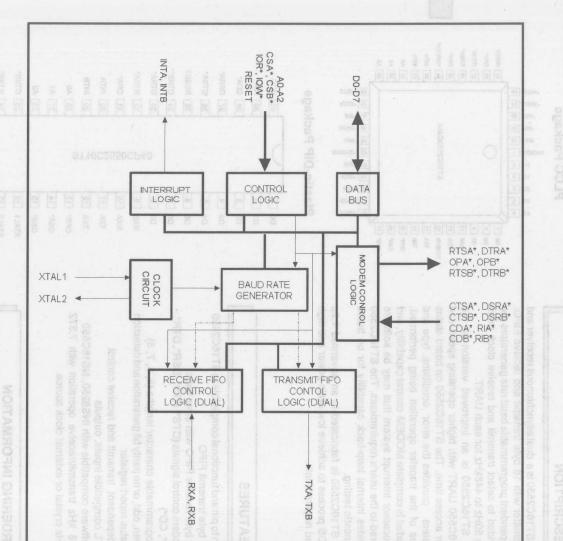


Plastic-DIP Package



3

BLOCK DIAGRAM



3-148

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	1-8	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B	10,9	and A bits. List yets ready Control of this put List take this put and have now or	Serial data input A/B. The serial information (data) received from serial port to ST16C2550 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B	11,12	O AM CART (AM CAM CAM CAM CAM CAM CAM CAM CAM CAM C	Serial data output A/B. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS A/B*	14,15 Sie	be sellto high florine resell high a the beasant o	Chip select A/B. (active low) A low at this pin enables the ST16C2550 / CPU data transfer operation.
XTAL1	16 word in Internation with the Internation of Internation Interna	l (auther of the control of the cont	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	17	ar noits f ol leann	Crystal input 2 or buffered clock output. See XTAL1.
IOW*	18	sifi =qq evisas	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	21	tis ead to each	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C2550 data bus to the CPU.
A0-A2	28-26	1	Address select lines. To select internal registers.
INT A/B	30,29	ti Albandine de la	Interrupt output A/B. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
0 is the least		a data Ous. Eigh imation to or fit it of the data bu or transmitted.	Interrupt enable output (active low). This pin stays high when INT out pin is set to three state mode and goes low when INT pin is enabled via OP2*. See bit-3 modem control register (MCR bit-3).
ircuit. A mark ro. During the from external ritemally.		nputA/O The serion to \$.7160 254 cone and a space ock mode the RX-and connected to \$	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR A/B* TT at a control of the cont	top. 48,88 my badding reset, 1 der is disabled. A low at this part operation.	output A/B. The additio Oil start, in the care, the transmit han the transmit A/B. (active low a CPU data transmit and a care.)	Data terminal ready A/B (active low). To indicate that ST16C2550 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
RESET is all a	ALZ p86 outility of the control of t	it 1 or external of this pln and XI roult. An external sit and baud rate	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
Il transfer the			Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
pin transfers	37,22 solid on this of out a bus to	the CPU data by I e. (active low) A s of the ST16C2	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD A/B* nentw) rigin es	38,19	ed lines. To se I put A/B. (active the interrupt en receive data a us condition flag	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem. Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description					
vcc	40	-4 Iba-3	Power supply input.					
GND	m qui 20	Oodum	Signal and power ground.					
TXRDY A/B	1,12**	0	Transmit ready. (active high) This pin goes high when the transmit FIFO of the ST16C550 is full. It can be used as a single or multi-transfer.					
RXRDY A/B*	34,23**	O person	Receive ready. (active low) This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.					

^{**} Available on the PLCC package only.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1 1	yfgme	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1 1	DER CTS data d	Line Control Register
100	0	0	a	Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0	are but bits bi	LSB of Divisor Latch
0	0	11		MSB of Divisor Latch
Ella	R-M	100	beers beers burt bu	At and at and At

ST16C2550 ACCESSIBLE REGISTERS A/B

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
ti n		r dgi	IER Is pin goes I Is full. It can	thigh) Th	O of the S	sen finnan	aT sti	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
n tr		V WO	FCR seop niq air lis as bear		RCVR trigger (LSB)	0 celve rea eive FIF0 ssier.	0 Re	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0	1	0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0	1	1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop	word length bit-1	word length bit-0
1	0	0	MCR	0	0	0	loop back	OP2/ INT enable	Not used	RTS*	DTR*
1.	0	1	LSR Register Register	-	trans. empty	trans. holding empty	break interrupt	framing	parity	overrun	receive data ready
1	1	0	MSR ster	0-1	Nodern	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1	1	1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	DLL dos	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

DLL and DLM are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

- A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.
- B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.
- C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C2550 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

- A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.
- C) LSR BIT-5 will indicate when the transmit FIFO is empty.
- D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.
- E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C2550 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C2550 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2¹⁶ -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:

0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1; ena nettimenent bors naviscent enti sonia

0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2: great as good as the so like 0-TIB 98.1 (A

0=disable the receiver line status interrupt.

IER BIT-3:

0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 4-7:

All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C2550 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C2550 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level was vid at anibivio one sHM 8-00 mon

Р	D3	D2	D1	D0	Source of the interrupt
13	0	1	1	0	LSR (Receiver Line Sta- tus Register)
2	0	1	0	0	tus Register) RXRDY (Received Data Ready)
2*	1	1(5)	0	0	RXRDY (Received Data time out)
3	0	0	es1m	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modern Status Register)

*RECEIVE TIME-OUT:

This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:

T = 4 X 7(programmed word length) +12 = 40 bits

Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:

T = 4 X 7(programmed word length) + 12 = 40 bits

Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

1=no interrupt pending.

ISR BIT 1-3: Izwollot as tuppo liw tour

Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7; a becase and livelif, level report terrimono

These bits are not used and are set to zero in ST16C450 mode. BIT 6-7: are set to "1" in ST16C2550 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:

0=Disable the transmit and receive FIFO.

1=Enable the transmit and receive FIFO.

This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:

0=No change.

1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:

0=No change.

1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:

0=No change.

1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":

When ST16C2550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":

When ST16C2550 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":

When ST16C2550 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":

When ST16C2550 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:

Not used.

FCR BIT 6-7:

These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	T-4 solects	bit Is er 10 ted, LCP Bit
0	1	04
eu 1 nun	0 0 0	inty is g 80 rated by for
of 1 Joer	o ball nevir	eth ethio be14 harest e

LINE CONTROL REGISTER (LCR) and a should

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0: 17/14/19 7 - 1-19 90 J by a 1 = 2-119 90

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
1.000	0	(T) fugiue 5 temens d
0	1	tan 6 at notice
1	0	7
1	1	8

LCR BIT-2:

The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3: of reacht and list of beau and affid speniil

Parity or no parity can be selected via this bit.

1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.

0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.

1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:s of beau at retained fording and entitle

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.

LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:

Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).

0=normal operating condition.

1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:

The internal baud rate counter latch enable (DLAB). 0=normal operation.

1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:

0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:

0=force RTS* output to high. 1=force RTS* output to low.

MCR BIT-2: 314 timens facility at nation and area (0=1)

Not used except in local loop-back mode.

MCR BIT-3:

0=set INT output pin to three state mode and OP2* output to high.

1=set INT output pin to normal operating mode and OP2* output to low.

MCR BIT-4:

0=normal operating mode.

1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and OP2*/INT enable are connected to modem control inputs.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:

Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0://OW TENSOR MANAGEMENT & CARSON TE

0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:

0=no overrun error (normal).

1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:

0=no parity error (normal).

1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:

0=no framing error (normal).

1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:

0=no break condition (normal).

1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:

0=transmit holding register is full. ST16C2550 will not accept any data for transmission.

1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:

0=transmitter holding and shift registers are full. 1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:

This bit is equivalent to OPZVIST enable. lamoN=01

1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:

Indicates that the CTS* input to the ST16C2550 has changed state since the last time it was read.

MSR BIT-1:

Indicates that the DSR* input to the ST16C2550 has changed state since the last time it was read.

MSR BIT-2:

Indicates that the RI* input to the ST16C2550 has changed from a low to a high state.

MSR BIT-3:

Indicates that the CD* input to the ST16C2550 has changed state since the last time it was read.

MSR BIT-4:

This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:

This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:

This bit is equivalent to MCR bit-2during local loop-back mode. It is the compliment of the RI* input.

3

MSR BIT-7:

This bit is equivalent to OP2*/INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C2550 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

16 x CLOCK DIVISOR	% ERROR
2304	:1-718 98
1536	dicates that ti
1047	0.026
857	0.058
768	S-TIS 98
384 9	dicates that t
192	s most beene
96	
48	SR BIT-3:
11 of 18 32 00 an	dicates that I
24	state begins
16	
12	SR BIT-4:
aleid to 8TS in the	ris bit is equiv
It is ite comple	bom sped-ge
2	2.77
1.	
	2304 1536 1047 857 768 384 192 96 48 32 24 16 12 6

ST16C2550 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR englading	LCR BITS 0-7=0
MCR SO	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0,
noletely receive	LSR BITS 5-6=1 LSR, BIT 7=0
MSR	the state of the s
ransferred to the	MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

SIGNALS	RESET STATE			
TX em lo co	High bereds entire			
OP2*	High			
RTS*	High			
DTR*	High (smon) tons			
VINTombib als	Three state mode			

AC ELECTRICAL CHARACTERISTICS

 $T_A = 0^{\circ} - 70^{\circ}$ C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
T,	Clock high pulse duration	50			ns	
T ₂	Clock low pulse duration	50	BOTTE		ns	External clock
T ₁ T ₂ T ₃ T ₈ T ₉	Clock rise/fall time			10	ns	
T ₈	Chip select setup time	5	evasetto		ns	=J - 16° 0, Voc≈51
T ₉	Chip select hold time	0			ns	
T,,	Data set up time	15			ns	
Table	Data hold time	15			ns	ladmy i
	IOW* delay from chip select	10			ns	
1 15	IOW* strobe width	50			ns	
16	Chip select hold time from IOW*	0			ns	Visit Comming
T ₁₇	Write cycle delay	55			ns	V _{ee} Cracking
Tw	Write cycle=T ₁₅ +T ₁₇	105			ns	wat tuggi . "V
T ₁₉	Data hold time	15			ns	Igin too a V
T ₂₁	IOR* delay from chip select	10	- 81U		ns	of teating
T	IOR* strobe width	65			ns	in highest 17
1 24	Chip select hold time from IOR*	0			ns	woo and the
T ₂₅	Read cycle delay	55			ns	roet hour least
Tr	Read cycle=T ₂₃ +T ₂₅	115			ns	Clock los
T ₂₆	Delay from IOR* to data			35	ns	100 pF load
T ₂₈	Delay from IOW* to output			50	ns	100 pF load
T ₂₉	Delay to set interrupt from MODEM input			70	ns	100 pF load
T ₃₀	Delay to reset interrupt from IOR*			70	ns	100 pF load
T ₃₁	Delay from stop to set interrupt			1 _{Rclk}	ns	100 pF load
T ₃₂	Delay from IOR* to reset interrupt			200	ns	100 pF load
T ₃₃	Delay from initial INT reset to transmit start	8		24	*	
T ₃₄	Delay from stop to interrupt			100	ns	
T	Delay from IOW* to reset interrupt			175	ns	
1,44	Delay from stop to set RxRdy			1 _{RCLK}		
15	Delay from IOR* to reset RxRdy			1	μS	
46	Delay from IOW* to set TxRdy			195	ns	
T ₄₇	Delay from start to reset TxRdy			8	*	
N	Baud rate devisor	1		216-1	÷	

Note 1: * = Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

Supply range
Voltage at any pin
Operating temperature
Storage temperature
Package dissipation

GND-0.3 V to VCC+0.3 V

0° C to +70° C

-40° C to +150° C

500 mW

DC ELECTRICAL CHARACTERISTICS

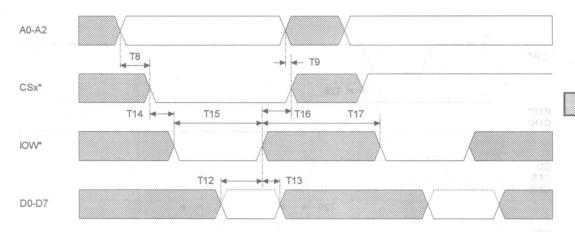
 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditio	ns
VILCK VIHCK VIL VIH VOL VOH ICC IIL ICL	Clock input low level Clock input high level Input low level Input high level Output low level on all outputs Output high level Avg. power supply current Input leakage Clock leakage	-0.5 3.0 -0.5 2.2 2.4	6 0	0.6 VCC 0.8 VCC 0.4 ±10 ±10	V V V V mA μA	one children with a control of the c	
bs	79 ns 100 pF lo	MEC		most to	set interru	Delay to input	- 65

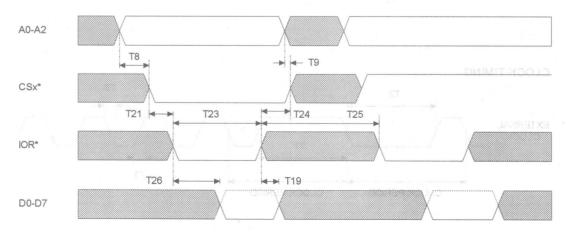
Baud rate devisor

3

GENERAL WRITE TIMING

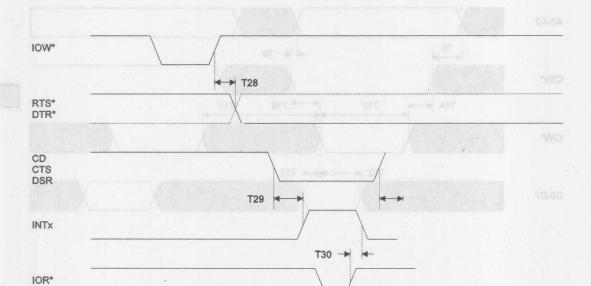


GENERAL READ TIMING

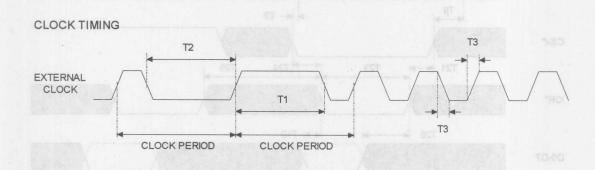


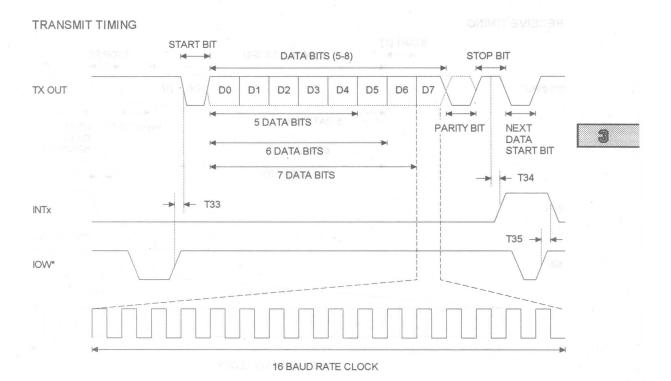
3-161

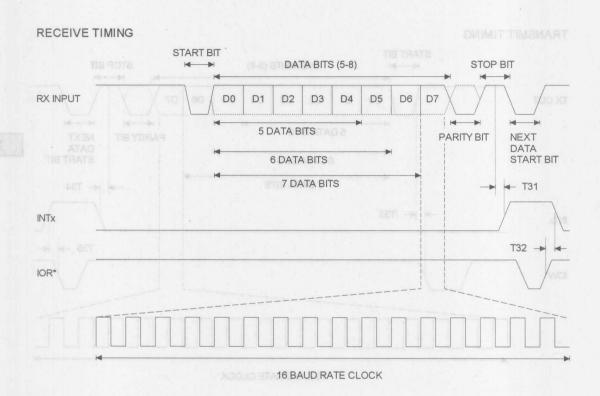
MODEM TIMING



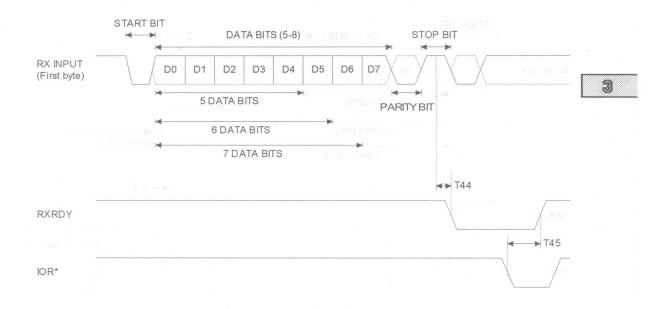
IS GENERAL READ TIMING



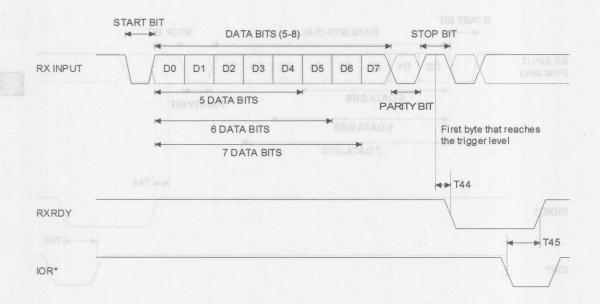




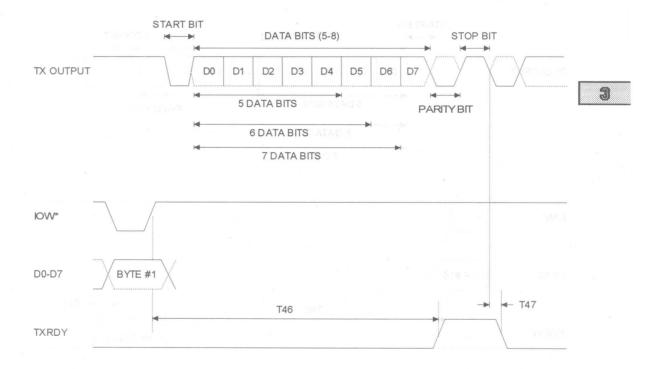
RXRDY TIMING FOR MODE "0"



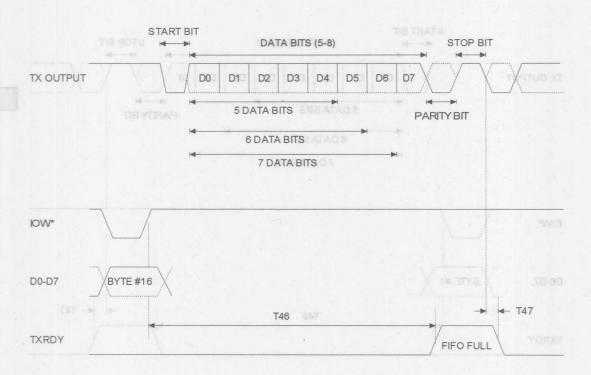
RXRDY TIMING FOR MODE "1"



TXRDY TIMING FOR MODE "0"



TXRDY TIMING FOR MODE "1"





ST16C2552

Printed September 7, 1994

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

DESCRIPTION

The ST16C2552 is a dual asynchronous receiver and transmitter with 16 byte transmit and receive FIFOs. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50Hz to 448kHz for each UART.

The on board status registers of the ST16C2552 provide the error conditions, type and status of the transfer operation being performed. Complete MODEM control capability and a processor interrupt system that may be software tailored to the user's requirements are included. The ST16C2552 provides internal loop-back capability for on board diagnostic testing.

Signalling for DMA transfers is done through two pins per channel (TXRDY, RXRDY*). The RXRDY* function is multiplexed on one pin with the OP2* and BAUDOUT functions. CPU can select these functions through the Alternate Function Register.

The ST16C2552 is fabricated in an advanced 1.2μ CMOS process to achieve low power and high speed requirements.

FEATURES

- Pin to pin and functional compatible to National NS16C552
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI* (CD*)
- Programmable character lengths (5, 6, 7, 8) bits
- Even, odd, or no parity bit generation and detection
- Status report register
- TTL compatible inputs, outputs
- Independent transmit and receive control
- Software compatible with INS8250, NS16C550
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

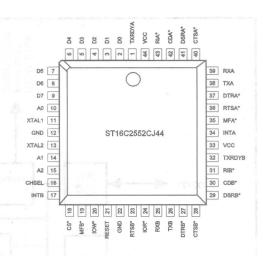
ORDERING INFORMATION

Part number ST16C2552CJ44 ST16C2552IJ44

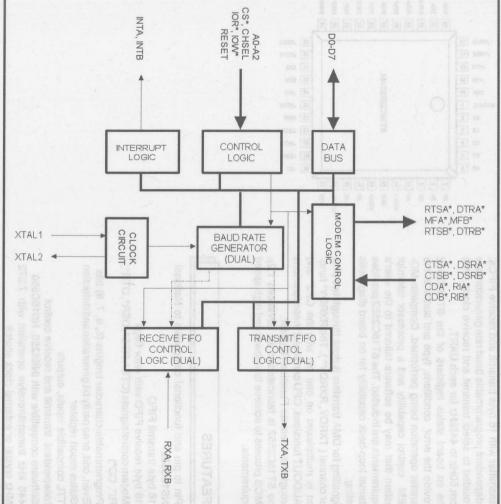
Package PLCC PLCC Operating temperature 0° C to + 70° C

-40° C to + 85° C

PLCC Package







Symbol	Pin	Signal Type	Pin Description
D0-D7 (4) (1) (2) (4)	2-9 10 12 2-9 10 10 10 10 10 10 10 10 10 10 10 10 10	otput OVI (British y the h tempt of w scent Broads after condition for	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B	39,25 CU	mint en poie). La buts see multiple in disput enable when this purisput hen this purisput Citchen, When	Serial data input A/B. The serial information (data) received from serial port to ST16C2552 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B mg	38,26	VERO DOUGH	Serial data output A/B. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	18 ** Bedg mg mill (m	l l l l l l l l l l l l l l l l l l l	Chip select. (active low) A low at this pin enables the ST16C2552 / CPU data transfer operation.
CHSEL	16	o send A/P is	UART A/B select. UART A or B can be selected by changing the state of this pin when CS* is active. Low on this pin, selects the UART B and high on this pin selects UART A section.
XTAL1 me and	iec liw 11 bd 20 of fac all linw no nations of before	yns awn i kin sa y sir i mwn o'u n e sir i mwe any	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	(adlevina) T		Crystal input 2 or buffered clock output. See XTAL1. Should be left open if a clock is connected to XTAL1.
IOW* 0 A 40	1020 stella	after the reset	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	24	et. (active myh.) d kmemal registr	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C2552 data bus to the CPU.
A0-A2	10,14,15	action I all be a	The state of the s

Symbol	Pin	Signal Type	Pin Description
	34,17d mg	formation to or	Interrupt output A/B. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
circuit. A mark sec. During the diffrom external internality. Internality of the TX will local loopback	stop and parity te during reset, litter is disabled.	port to ST 16C2 gloone and a spa lack mode the R2 and connected a output A/B. The hadditional staff mark (high) sta when the transm	OP2* (interrupt enable), BAUDOUT* and RXRDY* outputs. These outputs are multiplexed via Alternate Function Register. When output enable function is selected the MF* pin stays high when INT out pin is set to three state mode and goes low when INT pin is enabled. See bit-3 modem control register (MCR bit-3). When BAUDOUT function is selected, the 16 X TX/RX Baud rate clock output is generated. RXRDY function can be selected to use to request a DMA transfer of data from the Receive data FIFO. OP2* is the default signal and it is selected immediately after master reset or power-up.
TXRDY A/B	note 1,32	12 / CFO data to select. UART Av	Transmit ready. (active high) This pin goes high when the transmit FIFO of the ST16C2552 is full. It can be used as a single or multi-transfer.
RTS A/B*	gh on this pin a 36,23 clock impub. A (TALZ pin to util the clock can be use relicious can be	UART B and a vit f or external to this pin and and arough. An extern	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
	37,27 tiguo alogic berbed occupated berbed occupated by the connected by the control occupated b	left open if a cli ca. (active low) / I the CPU date.	Data terminal ready A/B (active low). To indicate that ST16C2552 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
RESET		be. (active low). ts of the ST f6C elect tines. To s	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.

Symbol Pin		Signal Type	Pin Description					
CTS A/B*	40,28	E-3+1 (-)	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be					
	nimentally a recent		tested by reading the MSR BIT-4. CTS* has no effect on the					
	publish enti-		transmit or receive operation.					
DOD A/Dt	status Legister	Agumelini.	B-tttt-A/B/c-tt					
DSR A/B*	41,29		Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin					
1 19214	RVDF THAN		does not have any effect on the transmit or receive opera-					
or Lane	SEO FEO		tion. sepphr spage!					
1	fessi i tessi		(38J) (18 ^t)					
CD A/B*	42,30		Carrier detect A/B (active low). A low on this pin indicates					
1 10	25 1 mi		the carrier has been detected by the modem.					
21.1613	priority pind lat		2011 PO11 P					
RI A/B*	C-110 43,31c no	i-iid	Ring detect indicator A/B (active low). A low on this pin indicates the modern has received a ringing signal from					
17 769	throw onto		telephone line.					
Total Co.	tipned Lint		so young blead nous					
VCC	33,44	1	Power supply input.					
GND	12,22	0	Signal and power ground.					

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0.00	0	0 5	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1 -	0 2 0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
110	0	0 000	bite 13 pite 12 bit 1 t	Modem Control Register
1	0	- 1	Line Status Register	
1	1	0	Modem Status Register	
-1°v	10-58	1 1-19:	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch
0	1	0	Alternate Function Register	Alternate Function Register

3

ST16C2552 ACCESSIBLE REGISTERS A/B

A2/	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
			n ellER TO		go eviso:	eer () bel	end	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0	1	0	FCR	RCVR trigger MSB)	RCVR trigger (LSB)	s no bay	0 0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 iq air		0	ne ISR edi	0/ FIFOs enabled	0/ FIFOs enabled	car0er h		int priority bit-2	int priority bit-1	int priority bit-0	int status
0	1	1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1	0	0	MCR	0 bn	101E 0 9W0	nai Ood p	loop back	OP2*	OP1*	RTS*	DTR*
1	0	.1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1	1	1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-10	bit-0
0	0	0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8
0	1	0	AFR	O gad Regit	0 Sorator	0	tus 0 egis Register		MF*	MF* sel-0	SP write

These registers are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

- A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.
- B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.
- C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1, resetting IER BIT 3-0 to zero puts the ST16C2552 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

- A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.
- B) LSR BIT4-1 will specify which error(s) has occurred.
- C) LSR BIT-5 will indicate when the transmit FIFO is empty.
- D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.
- E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR

Each UART section of the ST16C2552 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2¹⁶-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:

0=disable the receiver ready interrupt. 1=enable the receiver ready interrupt. 3

IER BIT-1:

0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2: ena patilmenant bas nevisoes entreoni?

0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3; aren't as long as there : E-TIB RS.1 (A

0=disable the modem status register interrupt. 1=enable the modem status register interrupt.

IER BIT 4-7:

All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C2552 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C2552 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level 10 and 1 to 29 -1. The or level year yet if

Р	D3	D2	D1	D0	Source of the interrupt
1	0	919	15	0	LSR (Receiver Line Status Register)
2	0	1 -(Я	0	0	RXRDY (Received Data Ready)
2*	1 onis	1 trax	0	0	RXRDY (Receive Data time out)
3	0	-	en 1 ni ejele	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

*RECEIVE TIME-OUT: WIND A TIME NA

This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be: $T = 4 \times 7$ (programmed word length) +12 = 40 bits Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be: $T = 4 \times 7$ (programmed word length) + 12 = 40 bits Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

1=no interrupt pending.

ISR BIT 1-3:

Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7: Detailed ad lived people beamage

These bits are not used and are set to zero if the FIFOs are not enabled. **BIT 6-7**; are set to "1" when the FIFOs are enabled.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:

0=Disable the transmit and receive FIFO. 1=Enable the transmit and receive FIFO.

FCR BIT-1: I shi to make hall show at his virtue set

0=No change, the previous for expects calls revisue

1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2: rate to vie unusion healthgrane u entre la 1 lo

0=No change.

1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3: 3-THE 90 I builden a sellid yining behilf

0=No change.

1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":

When ST16C2552 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":

When ST16C2552 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1": he asset as all

When ST16C2552 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":

When ST16C2552 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:

Not used.

FCR BIT 6-7:

These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0 (R)	DESCRIPTION OF THE PORTER IL
0	1	04
ecify t the	ga o 0 haar	ine Chilco80kgjister is a
		inconsula data benimunicani
		a tiel annula a discount for an analysis

ALTERNATE FUNCTION REGISTER (AFR) 8 903

This is a read/write register used to select specific modes of MF* operation and to allow both UART registers sets to be written concurrently.

AFR BIT-0:

When this bit is set, CPU can write concurrently to the same register in both UARTs. This function is intended to reduce the dual UART initialization time. It can be used by CPU when both channels are initialized to the same state. CPU can set or clear this bit by accessing either register set. When this bit is set the channel select pin still selects the channel to be accessed during read operation. Setting or clearing this bit has no effect on read operations.

The user should ensure that LCR Bit-7 of both channels are in the same state before executing a concurrent write to the registers at address 0,1, or 2.

AFR BIT 1-2: SV

Combinations of these bits selects one of the MF* functions.

BIT-2	BIT-1	MF* Function
0	0	OP2*
0	1	BAUDOUT*
1	0	RXRDY*
edf 101 (evel 1 egg	Reserved

AFR BIT 3-7:

Not used. All these bits are set to logic zero.

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0: RETEIGER MONTOMUR ETAMRET JA

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0 11	nem Ocnoc	is set, CFEI can write
0	ainditon is	sint at 76 I flod nin
ed (1so)	on One	satisitini 17 AU Isub s
eril 1 be	sitei1ni en	i when bol 8 oh annels a

LCR BIT-2: d of femants ent abeles life nio tosles

The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
HM1 erit	6,7,8	2 2

LCR BIT-3:

Parity or no parity can be selected via this bit. 0=no parity

1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4: en flids evision and 0 of one tentuco at

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.

0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.

1= EVEN parity bit is generated by forcing an even number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.

LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6: 1 = 0-lid 903) shorn 0313 srb nins (0=0

Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).

0=normal operating condition.

1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:

The internal baud rate counter latch enable (DLAB). 0=normal operation.

1=select Divisor Latch Register and Alternate Function Register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0: model ORFI firmenest entinenw (evilosni)

0=force DTR* output to high.

1=force DTR* output to low.

MCR BIT-1: nom 08808178 mi zi S88508178 medW

0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2: DOWN SUTTABLIAND STAN ON AS

Not used except in local loop-back mode.

MCR BIT-3:

0=force OP2* output to high. 1=force OP2* output to low.

MCR BIT-4:

0=normal operating mode.

1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:

Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:

0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:

0=no overrun error (normal).

1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:

0=no parity error (normal).

1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3: resw if amin'test of thomas its!

0=no framing error (normal).

1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

- 3

LSR BIT-4: 01 To only of hughl #GD ent

0=no break condition (normal).

1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:

0=transmit holding register is full. ST16C2552 will not accept any data for transmission.

1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:

0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7: Flow sales \$100 at his laving over 50 and

0=Normal. and at the automorphism de-

1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:

Indicates that the CTS* input to the ST16C2552 has changed state since the last time it was read.

MSR BIT-1: 0 got orld is relocated ord rifly betaloozes

Indicates that the DSR* input to the ST16C2552 has changed state since the last time it was read.

MSR BIT-2:

Indicates that the RI* input to the ST16C2552 has changed from a low to a high state.

MSR BIT-3:

Indicates that the CD* input to the ST16C2552 has changed state since the last time it was read.

MSR BIT-4: born Offfi of (smart emit relocated and

This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:

This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6: anelaiges Mida bots golblod settimanes =0

This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:

This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C2552 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	100 - 740 8310
75	1536	R BIT-4:
150	768	ntishede larmer
300	384	of issol sident
600	192	smitter output
1200	96	receiver input
2400	48	abled: Internet
4800	24	soon ent of belt
7200	16 Man	OP2" are out
	ush bridge viscer	
19.2K	at. The 6 odem.	fully operation
38.4K	rieff, but \$16 interr	also operation
	nabeM 211 to atid	
115.2K	Modemt Centrel	ead of the form

ST16C2552 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR and ale	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0,
rorFIFO.	LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, 1990 and 1990
	MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0
MFR	AFR BITS 0-7=0

SIGNALS	RESET STATE
er in the 'XT'	ster. Note the digit see
OP2*	High High
RTS*	High
DTR*	High
INT	Low
TxRdy	Low

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 7 Volts
Voltage at any pin GND-0.3 V to VCC+0.3 V
Operating temperature 0° C to +70° C
Storage temperature -40° C to +150° C
Package dissipation 500 mW

DC ELECTRICAL CHARACTERISTICS

 $T_A = 0^{\circ} - 70^{\circ} C$, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
V _{ILCK}	Clock input low level	-0.5	MARC	0.6	FILL VOTE	Churt selec
VIHCK	Clock input high level	3.0		VCC	V	HEAS DILLAN
V	Input low level	-0.5		0.8	V	Wifte eyel
V	Input high level	2.2		VCC	V	Data hold
V _{IL} V _{IH} V _{OL} V _{OH}	Output low level on all outputs			0.4	V	I _{oL} = 6 mA
VOH	Output high level	2.4			V	I _{OH} = -6 mA
Icc	Avg. power supply current	1	6	N 111011 8	mA	perati dirito
I	Input leakage	pc.		±10	μΑ	noyo naevi
I _{CL}	Clock leakage			±10	μА	NOÃO DRON

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ST16C2552

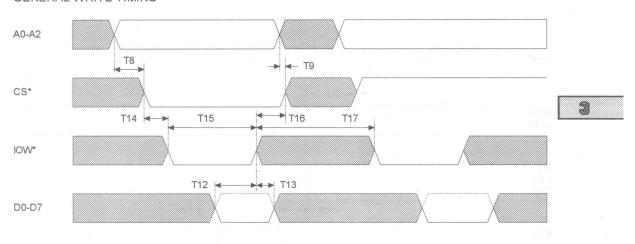
AC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

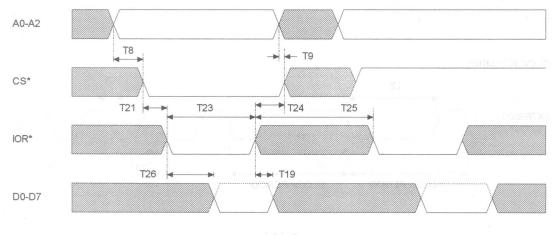
Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
T,	Clock high pulse duration	50			ns	
T.	Clock low pulse duration	50	ROITE	110000	ns	External clock
T.	Clock rise/fall time		COURT	10	ns	A TURNING A
T ₂ T ₃ T ₈ T ₉ T ₁₂	Chip select setup time	5			ns	
T.	Chip select hold time	5	Schelanize		ns	0° - 70° C, Vop=5.0
T.	Data set up time	15			ns	
T ₁₃ (101)	Data hold time	15			ns	
T ₁₄	IOW* delay from chip select	10			ns	lodmy
T ₁₅	IOW* strobe width	50			ns	
T ₁₆	Chip select hold time from IOW*	0			ns	
T ₁₇	Write cycle delay	55			ns	Vices Clock input
Tw	Write cycle=T ₁₅ +T ₁₇	105			ns	V _{HOK} Clock inpu
T ₁₉	Data hold time	15			ns	l wel jugal
T ₂₁	IOR* delay from chip select	10			ns	V _H Input high V
T ₂₃	IOR* strobe width	65	61		ns	100
T ₂₄	Chip select hold time from IOR*	0			ns	Voe Output hig
T ₂₅	Read cycle delay	55			ns	loo Avg. powel
Tr	Read cycle=T ₂₃ +T ₂₅	115			ns	In Input leaks
T ₂₆	Delay from IOR* to data			35	ns	100 pF load
T ₂₈	Delay from IOW* to output			50	ns	100 pF load
T ₂₉	Delay to set interrupt from MODEM input			70	ns	100 pF load
T ₃₀	Delay to reset interrupt from IOR*			70	ns	100 pF load
T ₃₁	Delay from stop to set interrupt			1 _{Rclk}	ns	100 pF load
T ₃₂	Delay from IOR* to reset interrupt		J. N. F.	200	ns	100 pF load
T ₃₃	Delay from initial INT reset to transmit start	8		24	*	
T ₃₄	Delay from stop to interrupt			100	ns	
T ₃₅	Delay from IOW* to reset interrupt		1 84 3	175	ns	
T ₃₆	Delay from initial Write to interrupt	16		24	*	
T.,	Delay from stop to set RxRdy			1 _{RCLK}		
T,5	Delay from IOR* to reset RxRdy			1	μS	MATERIAL PROPERTY.
46	Delay from IOW* to set TxRdy			195	ns	North North Co.
T ₄₇	Delay from start to reset TxRdy		, 1	8	*	
N	Baud rate devisor	. 1	214.5	216-1		

Note 1: * = Baudout* cycle

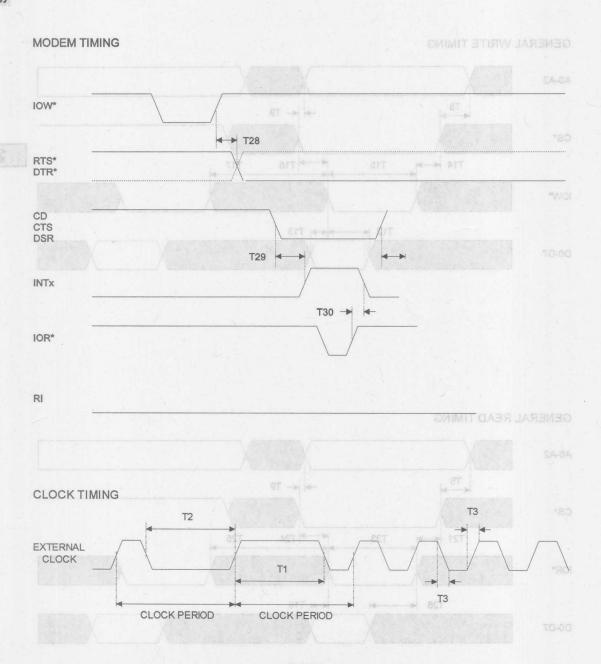
GENERAL WRITE TIMING

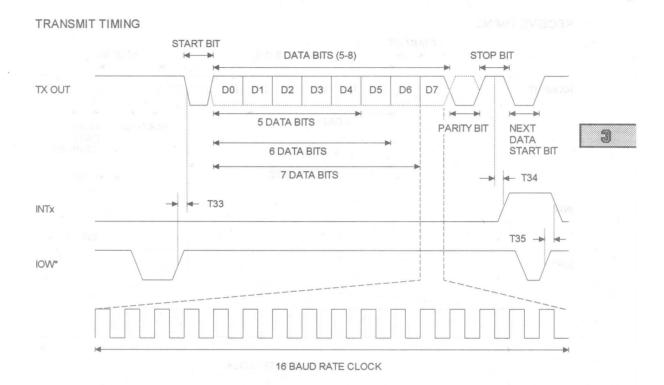


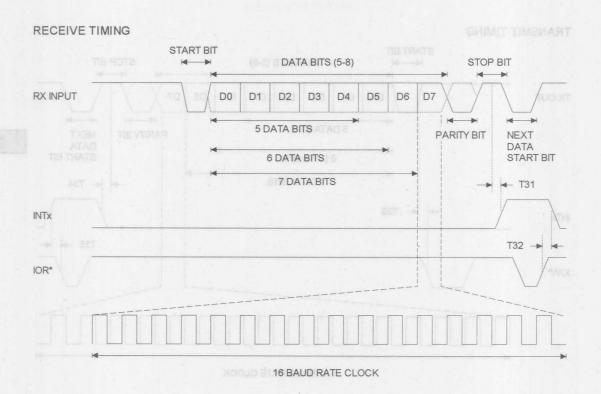
GENERAL READ TIMING



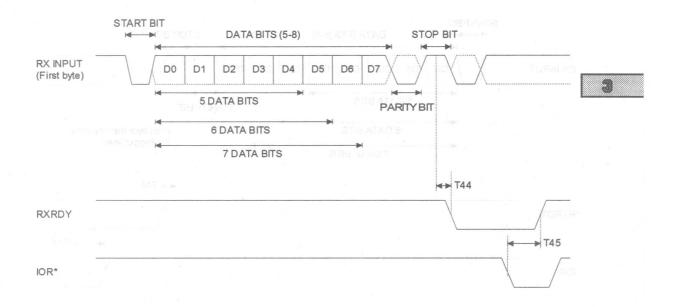
3-183



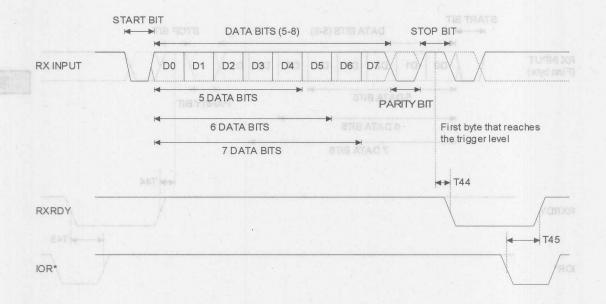




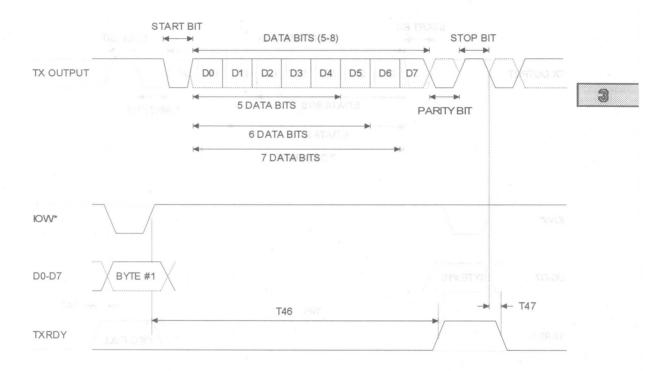
RXRDY TIMING FOR MODE "0"



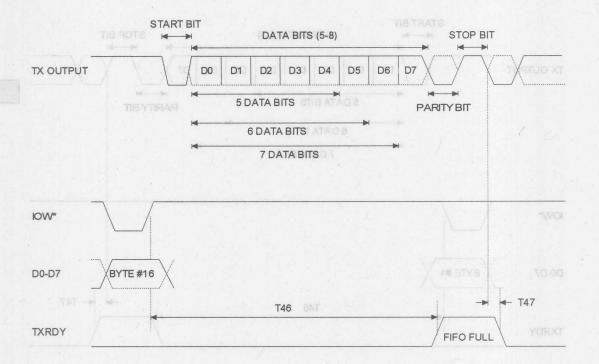
RXRDY TIMING FOR MODE "1"



TXRDY TIMING FOR MODE "0"



TXRDY TIMING FOR MODE "1"





Printed September 7, 1994

QUAD ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

DESCRIPTION

The ST16C554 is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C554 is an improved version of the NS16C550 UART with higher operating speed and lower access time. The ST16C554 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C554 provides internal loop-back capability for on board diagnostic testing.

The ST16C554 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

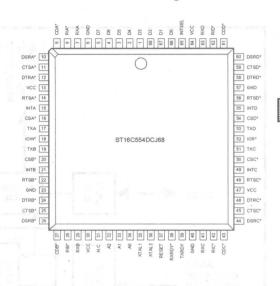
FEATURES

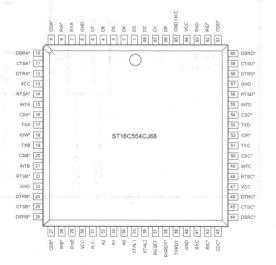
- Pin to pin and functional compatible to ST16C454
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- · Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C550
- 448 kHz transmit/receive operation with 7.372
 MHz crystal or external clock source

ORDERING INFORMATION

Part number	Package	Operating temperature
ST16C554CJ68	PLCC	0° C to + 70° C
ST16C554IJ68	PLCC	-40° C to + 85° C
ST16C554DCJ68	PLCC	0° C to + 70° C
ST16C554DIJ68	PLCC	-40° C to + 85° C

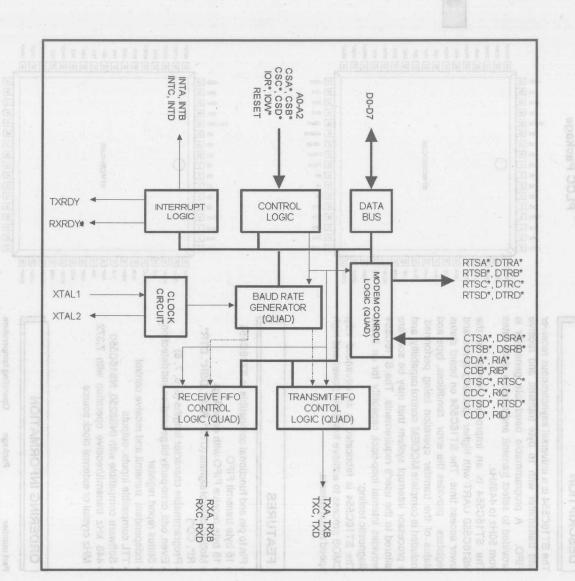
PLCC Package





8

BLOCK DIAGRAM



STAGESHO PARTS ONLY

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
a be in ed as a	554 te tuit. It oa	ady ONIVe high FO of the ST160 uith transier.	be received or transmitted.
RX A-B	7.29	E O L CA DHIN SQUI	10 BESTIDDA 1 35
RX C-D netal	ет Гаг 41,63 Говт. ет Гаптойн Гроге	elect lind 1, 10 a lect line 0, 10 a adv. (active high	from serial port to ST16C554 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external
		O is full, it can	Fi cytsget
TX A-B	17,19		nenstan
n benelected does no have	orugius igun CC (INCR bit-3	O ype setect. Enail tion. Normal but ting this pin to Y	in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
	1.4	on the intern	any effect
CS C-D*	50,541 80	utpulis selecte	Chip select. (active low) A low at this pin enables the ST16C554 / CPU data transfer operation. Each UART sections of the ST16C554 can be accessed independently.
XTAL1 evenesti su etgas talla	eble 35 star) a vallable, iranso j is determou.	ette condit in fla	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	off is 36 ft W	send, (active to-	Crystal input 2 or buffered clock output. See XTAL1.
to a low style	will set unis pin	Istor (MCR bit-1	Orystal input 2 of bullered clock output, See XTALT.
0.00.00	Manual 18 196 9	set tradpin with ave any effect of	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND GND	6,23 40,57	0	Signal and power ground.
fad" is ablight	of (wal svir	inal ready (a)	OTRICO 4655 O Dare term
IOR* SE TIG SE (Unit of ACING (Volume) ACING		is really to to via the moden streamCream	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C554 data bus to the CPU.

3

ST16C554/554D

Symbol	Pin	Signal Type	Pin Description
	in bit 98 ve sta rom the CPU II a and the first se	Action and the second second second	Transmit ready. (active high) This pin goes high when the transmit FIFO of the ST16C554 is full. It can be used as a single or multi-transfer.
A2	32	I I	Address select line 2. To select internal registers.
	33 177 18		Address select line 1. To select internal registers.
A0 partid on	solpol 34 of) so	ega s bris eno oi;	Address select line 0. To select internal registers.
RXRDY*	leidaaib ai lughi lugtuo 38 eri o	betoer O a bris	Receive ready. (active high) This pin goes high when the receive FIFO is full. It can be used as a single or multi-transfer.
INTSEL IIW XT no abom kos	reset, focel toppo bled. How at this pin	nol start, stop ar gir) state during enamitter is disc t. (active low)	Interrupt type select. Enable /disable the interrupt three state function. Normal interrupt output can be selected by connecting this pin to VCC (MCR bit-3 does not have any effect on the interrupt output). The three state interrupt output is selected when this pin is left open or connected to GND and MCR bit-3 is set to "1".
	49,55 A Jugat Accident of the colored can be also as a beautiful and selected can be also as a beautiful and as a selected can be also as a selected	the ST 18C554 c O ut if or external to this pin and it strough. An extern	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
RTS A-B* RTS C-D*	14,22 48,56	O but 2 or buffered se (active low) A	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR A-B* DTR C-D*	12,24 46,58	power ground. O se (active low) if	Data terminal ready. (active low) To indicate that ST16C554 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low.

^{**} ST16C554D PARTS ONLY

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
RESET	Tone 1 Services 1 Serv	neder 0 moder 0 salte state	This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation. Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and
CTS A-B* CTS C-D*	11,25 45,59	AMC 0 chars in th Officers State Officers State Officers Officers	the receiver input will be disabled during reset time. Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR A-B* DSR C-D*	10,26 44,60	yinsq nav.	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive opera-
CD A-B*	9,27	nop INT DROK LOBBY	tion. a a REM a a r
CD C-D*	43,61 8,28	yoak yaning coupt store	Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modern.
RI C-D*	42,62	etial 8T0	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC VCC	13,30 47,64	8 11.0 + 11.0	Power supply input.

9

ST16C554 ACCESSIBLE REGISTERS

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	1881	dqsi ion.	dig ains no d	set o Not semit or re nigh) A big	therone not the transition of	agiato or ny effect lasterresi	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0	1	0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	01 6	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
-	1	0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	ontro' fun seding the r receive	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0	sall	n inc	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop	word length bit-1	word length bit-0
1	0	0	MCR	0	0	0 .no	loop	INT enable	Not used	RTS*	DTR*
1	0	04 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
	1	0	MSR	CD	RI	DSR	стѕ	delta CD*	delta RI*	delta DSR*	delta CTS*
1	1	1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

DLL and DLM are accessible only when LCR bit-7 is set to "1".

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	3900	OT JES SIA SHE DESITION	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0	AUTATA TALISABINI	Modem Control Register
1	0	1	Line Status Register	THE PARTY BEGINSTLY TO SEPTEMBER
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0	nesonal respectations and the	LSB of Divisor Latch
0	0	1	Particeboom (ABP) and 1	MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

- A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.
- B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.
- C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C554 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

- A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.
- B) LSR BIT4-1 will specify which error(s) has occurred.
- C) LSR BIT-5 will indicate when the transmit FIFO is empty.
- LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.
- E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C554 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C554 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2¹⁶ -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:

0=disable the receiver ready interrupt. 1=enable the receiver ready interrupt.

IER BIT-1:

0=disable the transmitter empty interrupt. 1=enable the transmitter empty interrupt.

IER BIT-2:

0=disable the receiver line status interrupt. 1=enable the receiver line status interrupt.

IER BIT-3:

0=disable the modern status register interrupt. 1=enable the modern status register interrupt.

IER BIT 7-4:

All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C554 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C554 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

Р	D3	D2	D1	D0	Source of the interrupt
1	0	en ₁ bi (Ric	it Inc er (L)	0	LSR (Receiver Line Status Register)
2	0	ingin Jaiga	0	0	RXRDY (Received Data Ready)
2*	100	nibio	0	0	RXRDY (Receive Data time out)
3	0	0	ent i	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

*RECEIVE TIME-OUT:

This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:

T = 4 X 7(programmed word length) +12 = 40 bits

Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be: $T = 4 \times 7$ (programmed word length) + 12 = 40 bits Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

1=no interrupt pending.

ISR BIT 1-3: Parama sa aventa di didi potinoni Paramo

Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:

These bits are not used and are set to zero in ST16C450 mode. BIT 6-7: are set to "1" in ST16C554 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:

This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:

0=No change.

1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:

0=No change.

1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:

0=No change.

1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":

When ST16C554 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":

When ST16C554 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":

When ST16C554 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":

When ST16C554 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:

Not used.

FCR BIT 6-7: had be visual total A offs beat heytered

These bits are used to set the trigger level for the receiver FIFO interrupt.



	FIFO trigger level	BIT-6	BIT-7
15	nter logic 100 (the transp	nit si01 reg	0
8	d or eller 40 This bit w	I rebtm to	0
1	of the FIF 80	0	1
	14	- 1	1

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0: no lliw mig *YGRXT ent evitor and

These two bits specify the word length to be transmitted or received.

BIT-1 BIT-0		Word length
0	evioner	ast 1 ch 8 acter in the
0 7	CF et lev	will go Ico. Once act
e citaras	om On en	nactive) 7 han there
1	1	sceiver, 8

LCR BIT-2:bom 022021T2 mi ai 422021T2 nertW

The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)		
ld 900F	5,6,7,	8 mi. ai 1 -8808		
re tiftreor	trigger 2 vel or th	1-1/2		
onC1.wo	6,7,8	ache 2 the R		

LCR BIT-3:

Parity or no parity can be selected via this bit. 909 0=no parity

1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4: of browerd amshoro nearth: As elomaxe

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.

0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.

1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5: sale) + (f = fid gote) + (f = ythisg) + (T =

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.

LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:

Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).

0=normal operating condition.

1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7: "1" or see ers : 1-8 TIB : ebom 02AD81T8

The internal baud rate counter latch enable (DLAB). 0=normal operation.

1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0: III svieser bas timenest edt oldseiG=0

0=force DTR* output to high. Image of bloods and and 1=force DTR* output to low. See of bloods and and 1

MCR BIT-1:

0=force RTS* output to high. 1=force RTS* output to low.

MCR BIT-2: flids evisors with 0 of pipol retinuou ali

Not used, except in internal loop-back mode.

MCR BIT-3:

0=set the INT A-D output pin to three state mode.. 1=Enable the INT A-D output pin.

MCR BIT-4: 099 901 ASSMED STAN QUAR

0=normal operating mode. The State of Substitution of the substitu

1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and INT enable are connected to modem control inputs.

In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT 5-7:

Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:

0=no data in receive holding register or FIFO.

1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:

0=no overrun error (normal).

1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:

0=no parity error (normal).

1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:

0=no framing error (normal).

1=framing error received, received data did not have

a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:

0=no break condition (normal).

1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:

0=transmit holding register is full. ST16C554 will not accept any data for transmission.

1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6: thus send FAM of emisylups at fid at IT

0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In
FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:

0=Normal.

1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register

MSR BIT-0:

Indicates that the CTS* input to the ST16C554 has changed state since the last time it was read.

MSR BIT-1:

Indicates that the DSR* input to the ST16C554 has changed state since the last time it was read.

MSR BIT-2:

Indicates that the RI* input to the ST16C554 has changed from a low to a high state.

3

MSR BIT-3: shorts OFIF and all sid gots bliev as

Indicates that the CD* input to the ST16C554 has changed state since the last time it was read.

MSR BIT-4:

This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:

This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:

This bit is equivalent to MCR bit-2 during local loopback mode. It is the compliment of the RI* input.

MSR BIT-7: enerth end of the all fid airt ebert 0313

This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C554 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
	2304	
	1047	
150	768	231
300	384	his mode, the
600	192	fully operatio
1200	96	also operation
2400	48	rthe lower fau
4800	24	ead of the fo
7200	16	is are still out
9600	12	
19.2K	6	
38.4K	3	R BIT 6-ZI
56K	named 2 ex of la	2.77
115.2K	1	

ST16C554 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE		
IER OFFE TO THE	IER BITS 0-7=0		
ISR	ISR BIT-0=1, ISR BITS 1-7=0		
LCR	LCR BITS 0-7=0		
MCR	MCR BITS 0-7=0		
LSR	LSR BITS 0-4=0,		
	LSR BITS 5-6=1 LSR, BIT 7=0		
MSR	MSR BITS 0-3=0,		
ekisne ens 201	MSR BITS 4-7=input signals		
FCR	FCR BITS 0-7=0		

SIGNALS	RESET STATE		
TX	High		
RTS*	High (samen) 101		
DTR*	High		
RXRDY*	High and all most		
TXRDY	Low		
INT	Three state mode		

AC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
T, T,	Clock high pulse duration Clock low pulse duration	50 50	STICS	RETO	ns ns	External clock
T ₁ T ₂ T ₃ T ₈ T ₉	Clock rise/fall time Chip select setup time Chip select bold time	5 0	tweeter	10	ns ns	-0" - 70" C Véc=5
T ₁₂	Chip select hold time Data setup time Data hold time	15 15			ns ns ns	Symbol
T ₁₄ T ₁₅ T ₁₆ T ₁₇ TW T ₁₉ T ₂₁ T ₂₃ T ₂₄ T ₂₅ Tr T	IOW* delay from chip select IOW* strobe width Chip select hold time from IOW* Write cycle delay Write cycle=T ₁₅ +T ₁₇ Data hold time IOR* delay from chip select IOR* strobe width Chip select hold time from IOR* Read cycle delay Read cycle=T ₂₃ +T ₂₅ Delay from IOR* to data	10 50 0 55 105 15 10 65 0 55 115	200	25 100 06	ns ns ns ns ns ns ns ns ns ns ns	ani share o sa V sa
T ₂₈ T ₂₉	Delay from IOW* to output Delay to set interrupt from MODEM input Delay to reset interrupt from IOR*			50 70 70	ns ns	100 pF load 100 pF load 100 pF load
T ₃₀ T ₃₁ T ₃₂ T ₃₃	Delay form stop to set interrupt Delay from IOR* to reset interrupt Delay from initial INT reset to transmit start	8		1 _{Rclk} 200 24	ns ns ns	100 pF load 100 pF load
T ₃₄ T ₃₅ T ₄₄ T ₄₅ T ₄₆ T ₄₇	Delay from stop to interrupt Delay from IOW* to reset interrupt Delay from stop to set RxRdy Delay from IOR* to reset RxRdy Delay from IOW* to set TxRdy Delay from start to reset TxRdy			100 175 1 _{RCLK} 1 195 8	ns ns µs ns	
N	Baud rate devisor	1		216-1		

Note 1: * = Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

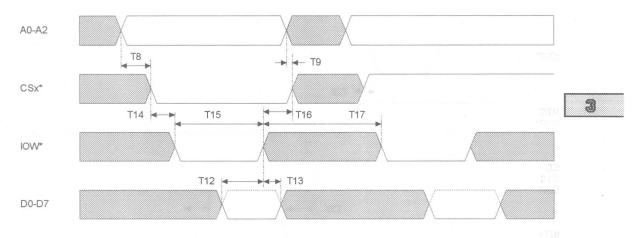
Supply range Voltage at any pin Operating temperature Storage temperature Package dissipation 7 Volts
GND-0.3 V to VCC+0.3 V
0° C to +70° C
-40° C to +150° C
500 mW

DC ELECTRICAL CHARACTERISTICS

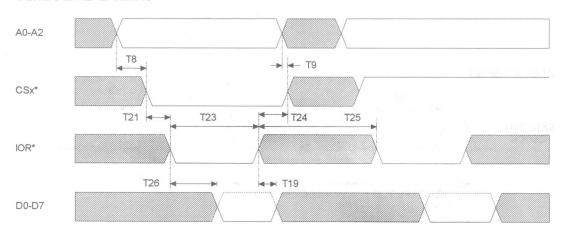
 $T_a=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

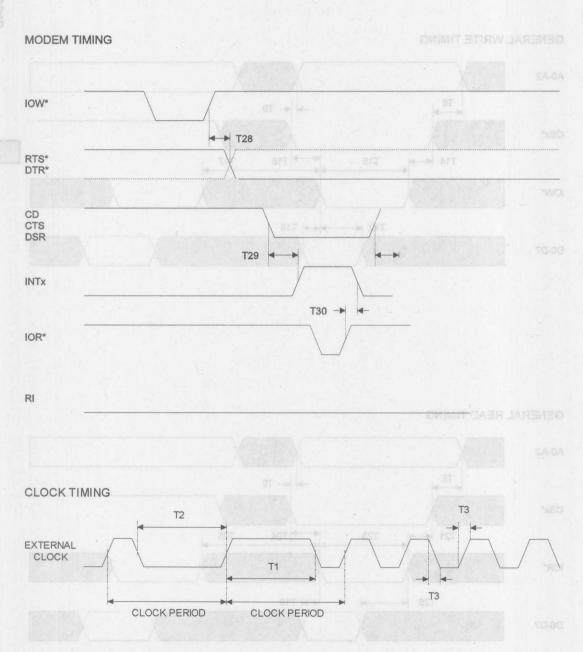
Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
V _{ILCK}	Clock input low level	-0.5	*WOI	0.6	V	T _{is} (OVV*-stn
VIHCK	Clock input high level	3.0		VCC	V	wa stata/
V	Input low level	-0.5		0.8	V	burn askalar urif
VIH	Input high level	2.2		VCC	V	don't stori
V _{OL} V _{OH}	Output low level on all outputs			0.4	V	$I_{ol} = 6 \text{ mA}$
VOH	Output high level	2.4		value dis	V	I _{OH} = -6 mA
I _{cc}	Avg power supply current		6	manit co	mA	sles oldo
I	Input leakage		2101	±10	μΑ	T Donal cur
ICL	Clock leakage	87		±10	μΑ	Tr Read ove
	35 ns 100 pF l			santa a		T Delay for

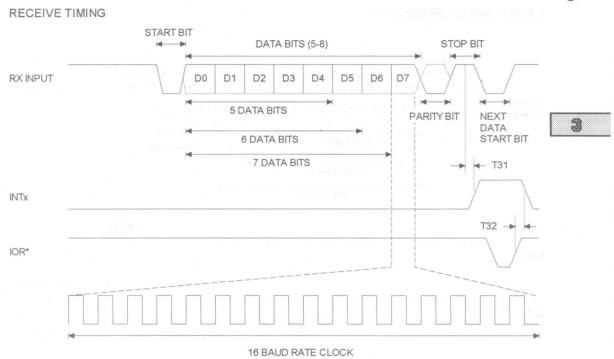
GENERAL WRITE TIMING



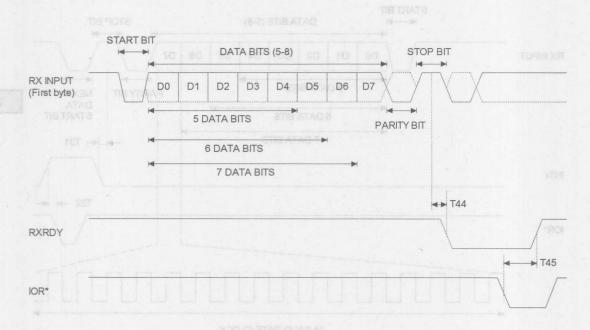
GENERAL READ TIMING



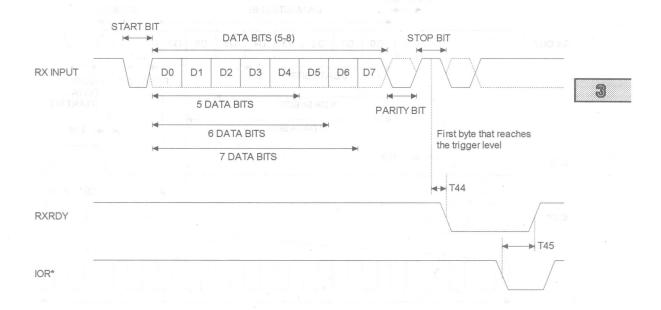


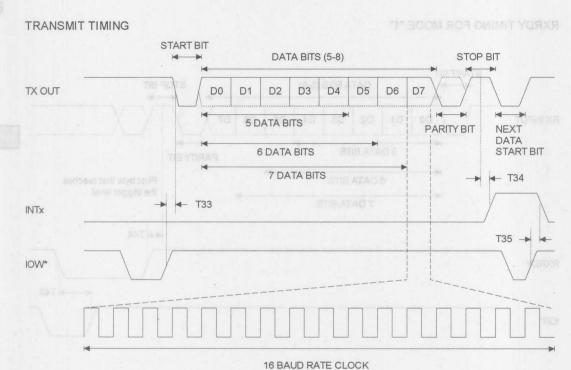


RXRDY TIMING FOR MODE "0"

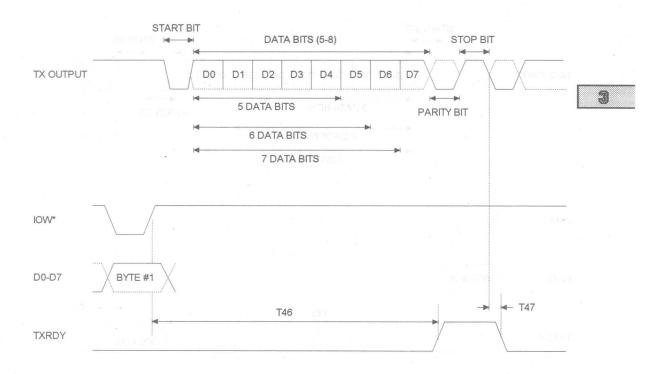


RXRDY TIMING FOR MODE "1"

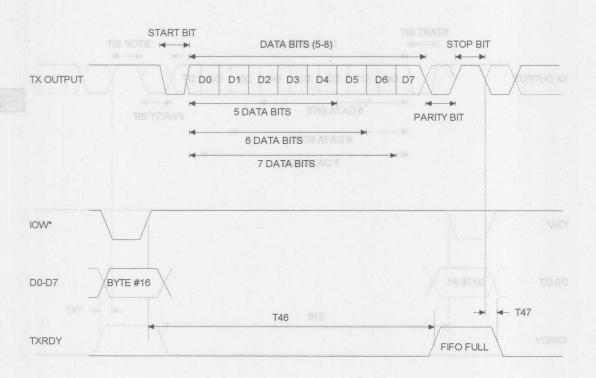




TXRDY TIMING FOR MODE "0"



TXRDY TIMING FOR MODE "1"





ST68C554

Printed September 7, 1994

QUAD ASYNCHRONOUS RECEIVER AND TRANSMITTER WITH FIFO

DESCRIPTION

The ST68C554 is a quad universal asynchronous receiver and transmitter with FIFO and modem control signals. Designed to interface with MOTOROLA, ROCKWELL, HITACHI bus and other popular microprocessors. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

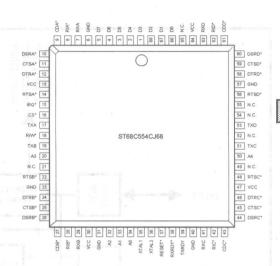
The ST68C554 is an improved, quad version of the NS16550 UART with faster operating access time. The on board status registers will provide the error conditions, type and status of the transfer operations being performed. Complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements to minimize the computing required to handle the communications link.

The ST68C554 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

FEATURES

- Motorola, Rockwell, Hitachi bus compatible
- Quad ST16C550
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*,RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- TTL compatible inputs, outputs
- 448 kHz transmit/receive operation with 7.372 MHz external clock source

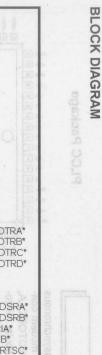
PLCC Package

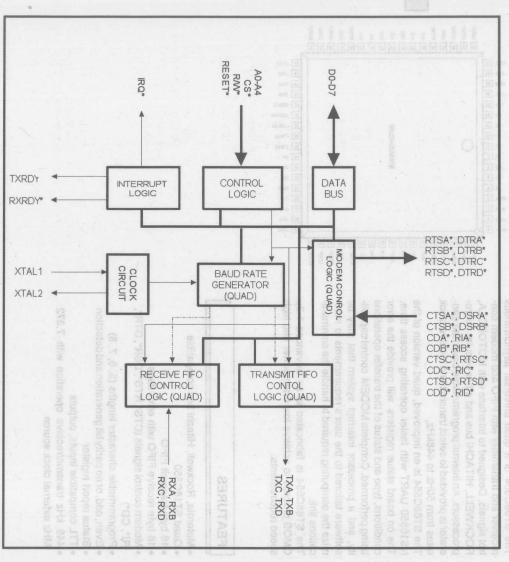


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ORDERING INFORMATION

Part number ST68C554CJ68 ST68C554IJ68 Package PLCC PLCC Operating temperature 0° C to +70° C -40° C to +85° C





3-214

Symbol	Pin	Signal Type	Pin Description
D7-D0	5-66 du a successión va sustata aposa da	OVI Heway lone,	Bi-directional data I/O. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B	7,29		85,3
RX C/D	41,63	A-D indexbyr at one ein cas ne se.	Serial data input. The serial information received from MODEM or RS232 to ST68C554 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
and the residence		end A-D (active	11 U/C* 48,56 O Requestres
TX A/B	17,19	Director to see s	lab dari rei
TX C/D	51,53 w	Table AOA) Team	german and comparing the contain and of contained it is
S 0 10 316 *8		SVIDS) C-A br	TRIC/D* 1 48,59 1 Olear to so
CS* carallett	16 W 18	ntest fu l arion la. Rollegrina MSR 8 Reput	Chip select (active low). A low at this pin will enable the UART A-D CPU data transfer operation.
XTAL1	35 U na salka e U na na na na	I S This secret or	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
V7410	lemal (gism s	I Z Talestonia	mil ara ibbA
XTAL2	36	1	Crystal input 2. See XTAL1.
R/W*	18		Read/Write strobe. A low on this pin will transfer the contents of the CPU data bus to the addressed register. A high on this pin will transfer the contents of the ST68C554 data bus to the CPU.
CD A/D*	0.07	Naol C. (36) Line	en inumatial O 80
CD A/B* CD C/D*	9,27 day 43,61	Nation of the lacest value of the lacest value of the lacest of the lacest value of th	Carrier detect A-D (active low). A low on this pin indicates that carrier has been detected by the modern.
GND	6,23,31		, 22-14
GND	40,57	0	Signal and power ground.
And a company of	CT As all to the sa	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	mmer et a C

Symbol	Pin	Signal Type	Pin Description
DSD A/D*	10.26	Incid Oli alab b	77-D0 5-66 VO Bi-direction
		at data I/O. Eigh	Data set ready A-D. (active low) A low on this pin indicates
			that MODEM is ready to exchange data with UART.
VO ATER ESSENT TERM	ou som one was	or transmitted.	
RI A/B*	8.28		7.29 P.A.XS
	nol.42,62m in C554 receive co. (tow) is logic ze	input. The sens RS232 to ST68 cone and a space	indicates that modem has received a ringing signal from telephone line.
		ck mode the RX	local loopba
		and connected to	
		output A. The via this pin with a	Request to send A-D. (active low) To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to low state. After the reset this pin will be set to high.
during reset,	rank (high) state	will be held in	Dits. The TX
		ck mode or whe	
	r operation.	(active low). A SPU data transfe	transmitter output.
		t 1 or external c	
		this ph and X	
		rouit. An external	
A3 amanan mea	210 TOT 20 19119	and blaud rate g	Address line 3. To select one of the four UARTS.
A2	32		Address line 2. To select internal registers.
	32	it 2. See XTAL	cini latevio
A1	33	1	Address line 1. To select internal registers.
transfer the	on this pin wil	strobe. A low	
		the CPU data but	
		pin will transfer to the CPU.	high on this
IRQ*	15	0	Interrupt output. (active low open collector) This pin goes low (when enabled by the interrupt enable register) when-
		ct A-D (active low has been detects	ever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected on UART A-D.
	2.7		3ND 6,23,31
DTR A/B*	12,24	cower ground.	SND 40,57 O Signal and
DTR C/D*	46,58	0	Data terminal ready A-D. (active low) To indicate that

Symbol	Pin	Signal Type	Pin Description
	'analg-9	Interrept Scales First Control Line Control Medem Cons	ST68C554 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset.
RESET*	37	bividita SIR I Dold to BEM	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
VCC VCC	13,30 47,64	1	Power supply input: 0230 JAMOITOMUR RATEIS
	runnen 39 gampo Locald Chill se present od fick in	t neilw LIRO er imed rigginte	Transmit ready (active high). This pin goes high when the transmit FIFO of the ST68C554 (any one) is full. It can be used as a single or multi-transfer DMA.
RXRDY*	the manuagate early 38, the early septification and early what and for	ia isRObjeto isvinari he Elic	Receive ready (active low). This pin goes low when the receive FIFO of the ST68C554 is full. It can be used as a single or multi-transfer DMA.

SERIAL PORT SELECTION GUIDE

e the receiver analog either un adon by er lizer	UART X	А3	A4	CS*
BUILDING WILLIAM	X	х	x	1
Ad they or I'm \$10	UART A	0	0	0
Office Visite	UART B	1	0	0
	UART C	0	1	0
SH LITTE 1 WHI	UART D	1	1	0

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PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	commoder via the modem con	Line Control Register
1	0	0	the S.	Modem Control Register
1	0	1.	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0	Master reset (active low) A low	LSB of Divisor Latch
0	0	1	- Walstell (Sound or low) A row	MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER A-D

The serial transmitter section consists of a Transmit Hold Register A-D and Transmit Shift Register A-D. The status of the transmit hold register is provided in the Line Status Register A-D. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A-D whenever the transmitter holding register A-D or transmitter shift register A-D is empty. The transmit holding register empty A-D flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A-D. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX A-D is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX A-D input. Receiver status codes will be posted in the Line Status Register A-D.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C)The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST68C554 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR

The ST68C554 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2¹⁶-1. Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER A-D

The Interrupt Enable Register A-D masks the incoming interrupts from receiver ready, transmitter empty, line status and modern status registers to the IRQ* output pin.

IER BIT-0:

0=disable the receiver ready interrupt
1=enable the receiver ready interrupt

IER BIT-1: 0g flav nig "YTTXXX and

0=disable transmitter empty interrupt
1=enable transmitter empty interrupt

IER BIT-2:

0=disable receiver line status interrupt 1=enable receiver line status interrupt

IER BIT-3: si, report and the of head are at

0=disable the modem status register interrupt
1=enable the modem status register interrupt

IER BIT 7-4:

All these bits are set to logic zero.

INTERRUPT STATUS REGISTER A-D

The ST68C554 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A-D provides the source of the interrupt in prioritized manner. During the read cycle, the ST68C554 pro-

vides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

Р	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
41	0	0	0	0	MSR (Modern Status Register)

*RECEIVE TIME-OUT: 91 bits filmanart ent aldea

This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:

T = 4 X 7(programmed word length) +12 = 40 bits

Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example-B: If user programs the word length = 7, with parity and one stop bit, the time out will be: $T = 4 \times 7$ (programmed word length) + 12 = 40 bits Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

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ISR BIT-0: was ad of lawer tournelini fee tour soft sable

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine

1=no interrupt pending

ISR BIT 1-2:

Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-5:

These bits are not used and are set zero.

ISR BIT 6-7:

0=Normal mode.

1=FIFO's are enabled.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:

0=Disable the transmit and receive FIFO.

1=Enable the transmit and receive FIFO.

FCR BIT-1:

0=No change.

1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:

0=No change.

1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3: How two error and Jid gots one boe vineg

0=No change.

1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

When ST68C554 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":

When ST68C554 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":

When ST68C554 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":

When ST68C554 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:

Not used.

FCR BIT 6-7:

These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	CIA RE	Talaan at 04 Ta Talin
top 1 stmil	0	decess of 80 destourleve
statt orin	vern1ad du	ons to minible software o

LINE CONTROL REGISTER A-DUTATE MECOM

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0: a user to it on revenue fit of its sia

These two bits specify the word length to be transmitted or received.

00=5 bits word length 01=6 bits word length 10=7 bits word length 11=8 bits word length

LCR BIT-2:

The number of stop bits can be specified by this bit.

0=1 stop bit, when word length=5, 6, 7, 8 bits
1=1 and 1/2 stop bit, when word length=5 bits
1=2 stop bits, word length=6, 7, 8 bits

LCR BIT-3:

Parity or no parity can be selected via this bit.
0=no parity

1=a parity bit is generated during the transmission; receiver also checks for received parity

LCR BIT-4:

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.

0=odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.

1=an even parity bit is generated by calculating the number of even 1's in the transmitted data; receiver also checks for same format.

LCR BIT-5:

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.

LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:

Break control bit.

1=forces the transmitter output (TX A-D) to go low to alert the communication terminal 0=normal operating condition

LCR BIT-7:ni bevus bac boyleger need can alab set

The internal baud rate counter latch enable (DLEN).
0=normal operation
1=select divisor latch register

MODEM CONTROL REGISTER A-D

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:

0=force DTR* output to high several phage 1=force DTR* output to low

MCR BIT-1:

0=force RTS* output to high ten) remains a mediane 0
1=force RTS* output to low and some prime in the prime i

MCR BIT2-3:

x=not used

MCR BIT -4: (4) Ignuiz Areald a havisper reviscer=1

0=normal operating mode ement and relocated and

1=enable local loop-back mode (diagnostics). The transmitter output (TX A-D) is set high (Mark condition), the Receiver inputs (RX A-D), CTS A-D*, DSR A-D*, CD A-D*, and RI A-D*) are disabled. Internally, the transmitter output is connected to the receiver input and DTR A-D*, RTS A-D* and MCR A-D bit-2,3 are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IER A-D.

MCR BIT 5-7: needs this and TOPIR entire noticeable

Not used. Are set to zero permanently.

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LINE STATUS REGISTER A-D

This register provides the status of data transfer to CPU. Op of (G-A XT) and the register and the status of data transfer to

LSR BIT-0:

0=no data in receive holding register
1=a data has been received and saved in the receive holding register

LSR BIT-1:

0=no overrun error (normal)

1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:

0=no parity error (normal)

1=parity error, received data does not have correct parity information

LSR BIT-3:

0=no framing error (normal) of higher (STS) solution

1=framing error received, received data did not have a valid stop bit

LSR BIT-4:

0=no break condition (normal)

1=receiver received a break signal (RX was low for one character time frame)

LSR BIT-5: doid tea at (C-A XT) tuetuo rettimenent

0=transmit holding register is full; ST68C554 will not accept any data for transmission

1=transmit holding register is empty; CPU can load the next character is departed in the next character is departed in the next character is departed in the next character in the next character is departed in the next character in the next character is departed in the next character in the next character is departed in the next character in the next character is departed in the next character in the next character is departed in the next character in the next character is departed in the next character in the next character in the next character is departed in the next character in the next character is departed in the next character in the next charac

LSR BIT-6: until retrimens to be revised and

0=transmitter holding and shift registers are full 1=transmitter holding and shift registers are empty

LSR BIT-7: if ent. Control Inputs. The in: The line is the control of the installation of the control of the co

0=Normal

1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER A-D

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:

Indicates that the CTS* input to the ST68C554 has changed state since the last time it was read.

MSR BIT-1:

Indicates that the DSR* input to the ST68C554 has changed state since the last time it was read.

MSR BIT-2:

Indicates that the RI* input to the ST68C554 has changed from a low to a high state.

MSR BIT-3: \(\dagger{0} \) dending dend browned with dots \(\text{\$1.5} \).

Indicates that the CD* input to the ST68C554 has changed state since the last time it was read.

MSR BIT-4:

This bit is equivalent to RTS in the MCR. It is the compliment of the CTS* input.

receiver also checks for received parity :5-TIB R2M

This bit is equivalent to DTR in the MCR. It is the compliment of the DSR* input.

0=odd parky is generated by calculating: 9-TIB 92M

This bit is equivalent to MCR bit-2 during local loopback mode. It is the compliment of the RI* input.

MSR BIT-7: betimened edimi e'i neve to redmun

This bit is equivalent to MCR bit-3 during local loopback mode. It is the compliment to the CD* input.

SCRATCHPAD REGISTER A-D and a viring and it

ST68C554 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16xCLOCK %ERROR	DVISOR		
50	2304	100 E 100		
75	1536			
150	768	and Admi		
300	384			
600	192	van til 3		
1200	96	100		
2400	48	tial of		
4800	24			
7200	16			
9600	12	0		
19.2	6	E T I I		
38.4K	3	5 11 1		
56K	2	2.77		
115.2K	1	tris D		

ST68C554 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER A-D ISR A-D	BITS 0-7=0 BIT-0=1, BIT-7=0
LCR A-D MCR A-D	BITS 0-7=0 BITS 0-7=0
LSR A-D	BITS 0-4=0, BITS 5-6=1, BIT-7=0
MSR A-D	BITS 0-3=0, BITS 4-7= input signals

SIGNALS	RESET STATE
TX A-D	High
RTS A-D*	High
DTR A-D*	High
RxRdy*	High
TxRdy	Low
IRQ	Three state mode

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ST68C554 ACCESSIBLE REGISTERS

											AR CILIA
A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0	1	0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0	1	0	ISR FIFOs	0/ FIFOs enabled	0/ enabled	0	0 priority	int priority bit-2	int priority bit-1	int status bit-0	int
0	1	1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1	0	0	MCR	0	0	0	loop back	Not used	Not used	RTS*	DTR*
1	0	1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity	overrun	receive data ready
1	1	0	MSR	CD	RI	DSR	стѕ	delta CD*	delta RI*	delta DSR*	delta CTS*
1	1	1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

DLL and DLM are accessible only when LCR bit-7 is set to "1".

AC ELECTRICAL CHARACTERISTICS

 $T_a=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
т	Clock high pulse duration	50			ns	
T_{1} T_{2} T_{3} T_{8} T_{9} T_{12}	Clock low pulse duration	50			ns	External clock
T ²	Clock rise/fall time	30	8.110.8	10	ns	LAternal Clock
T ³	Chip select setup time	5		10	ns	
_8 	Chip select setup time	ေရွိေး	divisatio		ns	=0 - 70 ° C, VdG=5
1 9	Data setup time	15			ns	
T 12	Data setup time Data hold time from write or CS*	15				
T ₁₃	Write set up time	10			ns ns	fodmy
114	Write strobe width	50				
T ₁₅	Chip select hold time from write	15			ns	
T ₁₆	Write cycle delay	45			ns ns	V . Clock into
T ₁₇	Data setup time	15	n		ns	oni zoolo N
T ₁₈ Tw	Write cycle=T ₁₅ +T ₁₇	105			116 v 91	wol Jugal V
	Data hold time	0			ns	V Input high
T ₂₄		25			ns	V _a Output to
T ₂₅ Tr	Read cycle delay	105			ns	
T . A	Read cycle=T ₁₈ +T ₂₅ Chip select pulse width	75			ns	V _m Output n
T ₂₇		/5		50	ns	100 pF lood
T ₂₈	Delay from Write to output				ns	100 pF load
T ₂₉	Delay to set interrupt from MODEM input			35	ns	100 pF load
T ₃₁	Delay from stop to set interrupt			1 _{Rclk}	ns	100 pF load
T ₃₂	Delay from Read to reset interrupt			200	ns	100 pF load
T ₃₃	Delay from initial IRQ* reset to transmit start	8		24	*	
T ₃₄	Delay from stop to interrupt			100	ns	
T ₃₅	Delay from Write to reset interrupt			75	ns	
1 77	Delay from stop to set RxRdy		v =	1 _{RCLK}		
T ₄₅	Delay from read (CS*) to reset RxRdy			1 RCLK	μs	
T ₄₆	Delay from write to set TxRdy			195	ns	
T ₄₇	Delay from start to reset TxRdy			8	*	

^{* =} Baudout* cycle



ABSOLUTE MAXIMUM RATINGS

Supply range
Voltage at any pin
Operating temperature
Storage temperature
Package dissipation

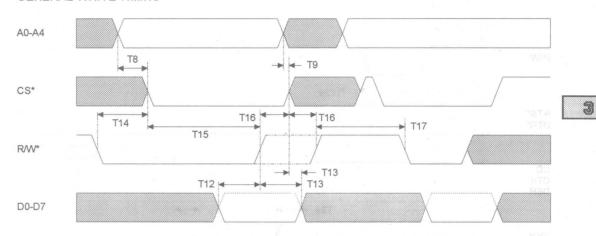
GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

DC ELECTRICAL CHARACTERISTICS

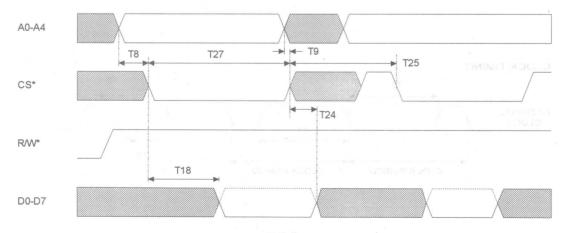
 T_A =0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Min Typ Max			Conditions
V _{ILCK}	Clock input low level	-0.5	Billion	0.6	V	Chip sele
VIHCK	Clock input high level	3.0		VCC	V	DVICE CYC
V _{II}	Input low level	-0.5		0.8	V	Bata setu
V.,	Input high level	2.2		VCC	V	I'w Write cyc
V _{IL} V _{IH} V _{OL}	Output low level	3		0.4	V	I _{oL} = 6 mA on all outputs
V _{OH}	Output high level	2.4		246.5	V	I _{OH} = -6 mA
I _{cc}	Avg. power supply		6	ritbii Juqtuo e	mA	Car Chip Son
I, ba	Input leakage		MEGON	±10	μА	Delay to
I _{CL}	Clock leakage		ious	±10	μА	Input L Delay fro

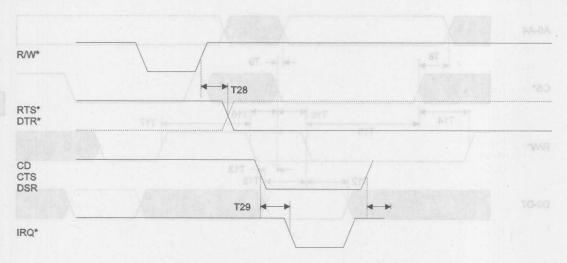
GENERAL WRITE TIMING



GENERAL READ TIMING



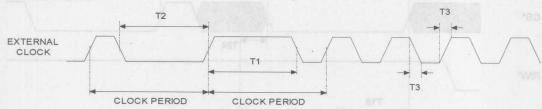


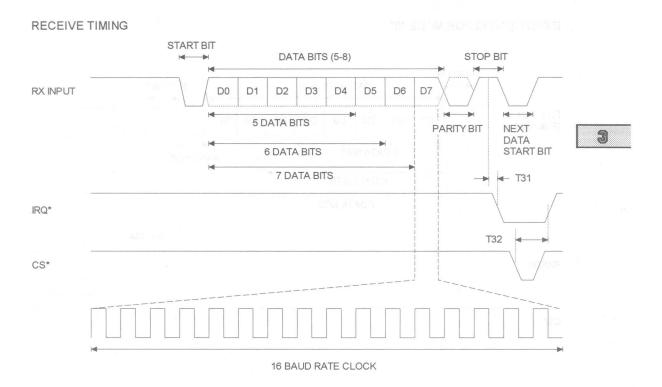


RI

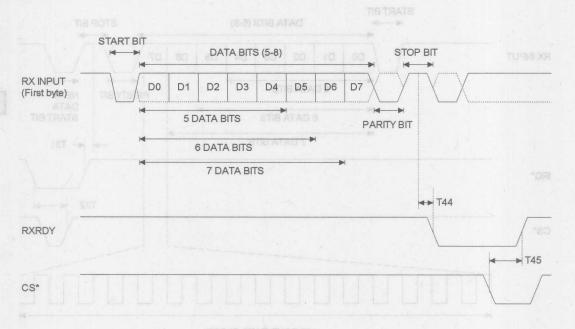
GENERAL KEAD TIMING

CLOCK TIMING

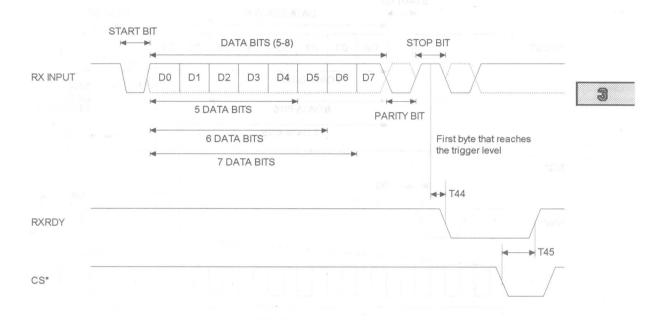


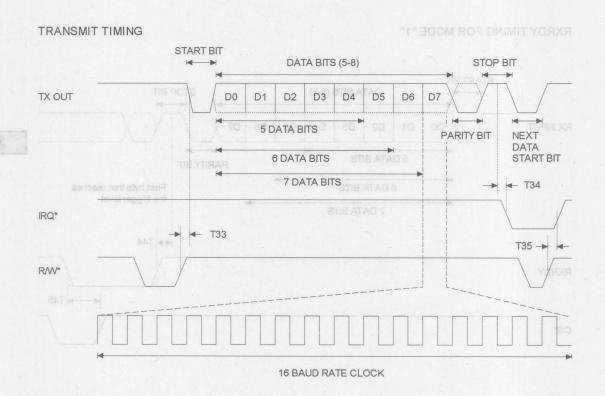


RXRDY TIMING FOR MODE "0"

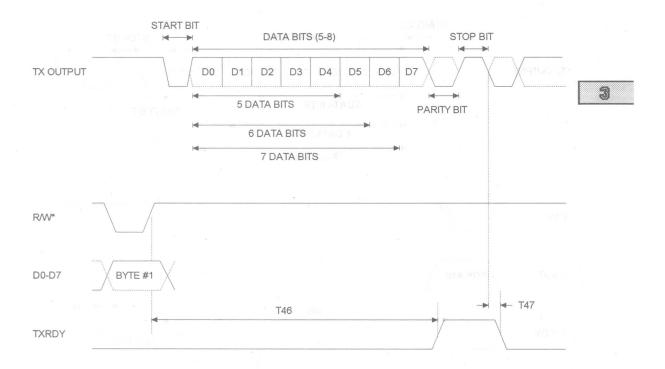


RXRDY TIMING FOR MODE "1"

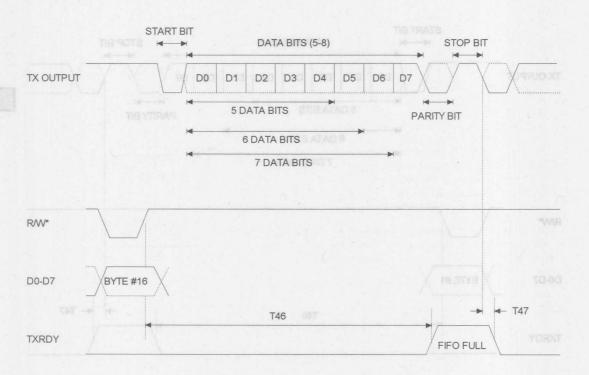




TXRDY TIMING FOR MODE "0"



TXRDY TIMING FOR MODE "1"





ST16C650

Printed September 8, 1994

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFO's

DESCRIPTION

The ST16C650 is a universal asynchronous receiver and transmitter with 32 bytes transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C650 is an improved version of the ST16C550 UART with deeper FIFO, software/ hardware flow control. The ST16C650 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C650 provides internal loop-back capability for on board diagnostic testing. The ST16C650 provides pin selectable interface mode to function as stand alone ST16C550 or direct PC connect.

The ST16C650 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

FEATURES

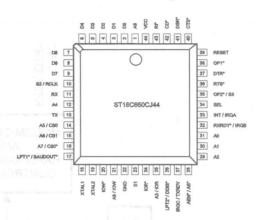
- Pin to pin and functional compatible to NS16550 VL16C550, WD16C550, ST16C550
- 32 byte transmit FIFO
- 32 byte receive FIFO with error flags
- · Pin selectable interface mode
- Software/Hardware flow control
- · Programmable Xon/Xoff characters
- Sleep mode (800μA stand-by)
- Low operating current (1.5mA typ.)
- Independent transmit and receive control
- 460 kHz transmit/receive operation
- Selectable Transmit/Receive trigger levels
- . Infrared receive and transmit, input / output.

ORDERING INFORMATION

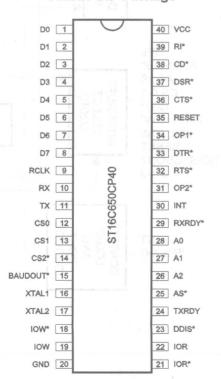
Part number	Package	Operating	temperature
ST16C650CP40	Plastic-DIP	0° C	to + 70° C
ST16C650CJ44	PLCC	0° C	to + 70° C
ST16C650CQ52	QFP	0° C	to + 70° C
ST16C650CQ48	TQFP	0° C	to + 70° C

*Industrial operating range are available

PLCC Package



Plastic-DIP Package

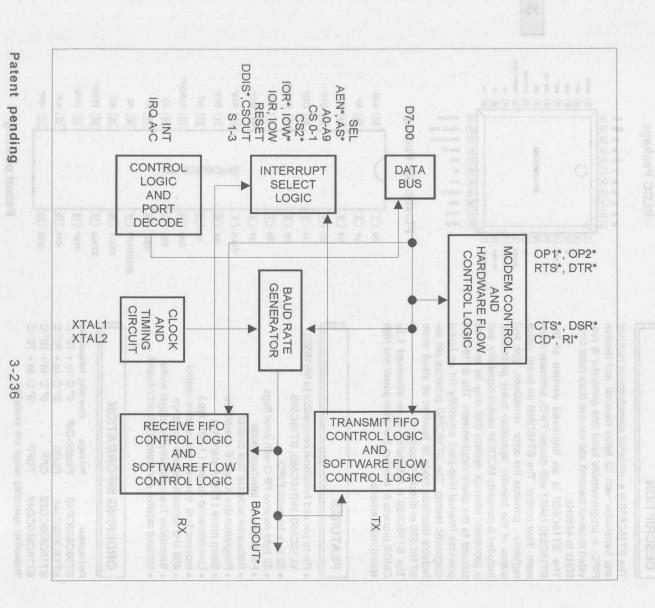


Patent pending

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BLOCK DIAGRAM





Symbol	rmbol Pin Signal Type		Address select line 9. When PC mode is selected, this pin is used as 10th address line to decode the standard COM1-4 ports.			
Agol annell (1 cont. 1 cont. 1 cont. 1 (1 cont. 1 cont		Tor Cipp resco enumer, this pro- enced Culphan				
D0-D7	2-9		Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.			
S2/RCLK	10	now soot ever and the vertical and the land which the land which the land to t	Port select-2 or Receive clock input (dual function). When PC mode is selected the RCLK input is connected internally to BAUDOUT* output pin and S2 is used to select one of the ComPort addresses (Com1-4). During STD mode operation, this pin is used as external clock input to the ST16C650 receiver section.			
1.045 F 168 J	HA OL KENTON USTOL 11 STORY OUTUS NOVE OF	rative to the	Serial data input. The serial information (data) received from serial port to ST16C650 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loop-back mode the RX input is disabled from external connection and connected to the TX output internally.			
A4 Short ened the	12 v riig e	I. A win sville) - k alla uraa sin	Address select line 4. When PC mode is selected, this pin is used as 5th address line to decode the standard COM1-4 ports.			
TX Table of the Carlos	of 13 liber or di2 es base papaci en l ordata secolo	Viete of Cores of Cor	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loop-back mode or when the transmitter is disabled.			
A5/CS0	14	ter unit 1 woo	Address line 5 or Chip select-1 (dual function). During the PC mode operation, this pin is used as 6th address line to decode the standard COM1-4 ports. During STD mode this pin acts as active high chip select input pin.			
A6/CS1	15 15 15 15 W	t best Tset t	Address line 6 or Chip select-2 (dual function). During the PC mode operation, this pin is used as 7th address line to decode the standard COM1-4 ports. During STD mode this pin acts as active high chip select input pin			

Symbol Pin Signal Type		Signal Type	Pin Description			
A7/CS2*, beta les at 16 m on month. If and come the state of the come			PC mode operation, this pin is used as 8th address line to decode the standard COM1-4 ports. During STD mode this pin acts as active low chip select input pin.			
BAUD/LPT1* a fel data bit to a fed internally a fed internally a fed one of the	om the first so and the first so k input (dual fu Xinput is conne \$2 is used to so	It of the data be or transmitted. 2 or Receive close selected the RCI T* output pin and	Baud rate generator clock output or LPT1 decode address (378 Hex) (dual function). This output provides the 16X clock of the internal selected baud rate during standard mode. RCLK pin is connected externally to BAUDOUT* pin to provide receive clock when STD mode is selected. This pin internally is connected to RCLK input and address 378 Hex is decoded when PC mode is selected.			
teta) received crouit. A mark	al cloc 81 por to	tion. Input. The sense on to ST16C65	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.			
nternally.	nput 19 Isable tine TX output	and connected t	Crystal input 2 or buffered clock output. See XTAL1. External 1 $M\Omega$ resistor is required to connect between XTAL1 and XTAL2 pins.			
lected, this ain and and and and and and and and and an	20	act line 4. When h eddor s line t	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.			
tack mode or on.		ultput. The sena ist start, stop and h) state during r insmitter is disal s 5 or Chip select	Address 8 or Write strobe (dual function). During the PC mode operation, this pin is used as 9th address line to decode the standard COM1-4 ports. During STD mode this pin functions as Write strobe (active high). Same as IOW*, but uses active high input. Note that only an active IOW* or IOW input is required to transfer data from CPU to ST16C650 during write operation.			
STD mode this		standard COM1-	Signal and power ground.			
oe) During th 12	olionui 23 liby c., o di 7 as beau a	6 or Chip selection, this pin	Port select-1. S1 is used to select one of the ComPort addresses (Com1-4).			
IOR*	nig 1, 24 (59)	standard COM1- active high chip	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C650 data bus to the CPU.			

Pin	Signal Type	Pin Description
	right (righs fund fluor, this pluse in rebien by inclina- fuer error, i ruelina indere steue institution	Address line 3 or Read strobe (dual function). When PC mode is selected, this pin is used as 4th address line to decode the standard COM1-4 ports. During STD mode operation this pin is used as Read strobe. Same as IOR*, but it is used as active high Read strobe. Note that only an active IOR* or IOR input is required to transfer data from ST16C650 to CPU during read operation.
26) - 3 () -	secret Ofernia obs. Tandas republikases Per	Drive disable or LPT2 decoded address (278 Hex) (dual function). (active low) This pin goes low when the CPU is reading data from the ST16C650 to disable the external transceiver or logic's during STD mode. During PC mode, LPT2 address is decoded.
27 anui leus du Irolae e suon e lac ei ance	Liste defined out	IRQ-C Interrupt (three state) or Transmit ready (dual function). Three state interrupt output during PC mode and Transmit ready during STD mode. When STD mode is selected this pin goes high when the transmit FIFO of the ST16C650 is full. See INTA/INT description for IRQ-C operation.
	1 0 90M na.s o the mg cit i the bolts yas sw Tulky bold or	Address enable or Address strobe (dual function). During PC mode operation Valid COM 1-4 ports are decoded when this pin goes low. A low on this pin During STD mode latches the state of the chip selects and addressed register (A2-A0). This input is used when signals are not stable for the duration of a read or write operation. If not required, tie the AS* input permanently low.
29	in read, in feet	Address select line 2. To select internal registers.
30	Taid OC Partie	Address select line 1. To select internal registers.
nio en 31	de la secolar de la secolar	Address select line 0. To select internal registers.
32 pediam ia e-	0	IRQ-B Interrupt (three state) or Receive ready (dual function). Three state interrupt output during PC mode and Receive ready during STD mode. During the STD mode operation this pin goes low when the receive FIFO is full. See INTA/INT description for IRQ-B operation.
	25	25

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
dress line to g STD mode eas IOR*, but that only an ifer data from the CPU is the external	4 ports. Durit ead strobe. San at strobe. Note equired to tran ad operation. ded address (2 in goes low whi coso to disabi	ected, this pin is standard COM spin is used as F active high Re or IOR input is to CRU during it is or LPT2 deceptive low) This particle in the STM.	IRQ-A Interrupt (normal, three state or open source) or Interrupt output (triple function active high). During PC mode operation, this pin is activated when MCR Bit-3 is set to "1" and enabled by the interrupt enable register. whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected. During the STD mode operation three state mode is disabled and functions as active IRQ-A. Multiple ST16C650 interrupts can be connected to form a wired "Ored" function by setting the MCR bit-5 to "1" and connecting a 450 Ω resistor to ground.
SEL dual func-	34 ser simener Tho	or logic's during as is deboded. rupt (three state)	Mode select (pulled-up). PC mode is selected by tying this pin to GND and STD mode is selected when this pin is left
\$3/OP2*1 CT2	med 25 Men meneral men	state interrupt edy dO/I g STE s pin goes high y is full. See INT	Select-3 or User defined output (dual function). ComPort
recoded when mode latches ister (A2-A0). stable for the	M 1-4 ports are i pin During STE nd addressed re- ignals are not	able to describe the control of the	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation it is not enabled via EFR Bit-6.
	lect internal reg	ect line 2. To se ect line 1. To se ect line 0. To se	Data terminal ready. (active low) To indicate that ST16C650 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
OP1* sbom O	gutpu88 umg 1 mode. During 1	rupt (three state) state Orterrupt ady during STD lis pin goes low	User defined output. See bit-2 of modem control register (MCR bit-2).
		NT desdription for	

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
	la resignal at es	CTS input challes	the receiver input will be disabled during reset time.
CTS* Unonega of or serious little of the equation of the encompact of the	40 Haza		Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation if it is not enabled via EFR Bit-7.
DSR* DSIds	e el 141 se di 16 e e e e e e e e e e e e e e e e e e	o cheration. Di 80650 will accept a	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD* of habit	42		Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modern.
RI*	43 recado un bang and aboni goule and and aboni es a 35 mes	STIGGE SQ is described in the choice and to the choice and to the choice and to the choice and to the choice and the choice an	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line. Power supply input.

DESCRIPTION OF NEW FEATURES

The ST16C650 is designed to upgrade the existing 16C550 market. It provides additional features to reduce the software over-head, external glue logic, operating and stand-by current, and maintain the 16C550 software compatibility with existing software's.

After reset ST16C650 is down-ward compatible with ST16C450 and ST16C550 except it provides 32 bytes of data FIFO (when ST16C550 mode is enabled) instead of 16 bytes. All other additional features are available through special function register. The 40 pin Dip package offers the software/Hardware flow control, sleep mode, selectable transmit trigger levels, and two selectable baud rate generators. The 44 pin

PLCC package offers all the above features with selectable dual foot print (direct PC connect), two additional three state interrupt lines, and one selectable open source interrupt output to "Or" other ST16C650 interrupt outputs to reduce the number of interrupt lines.

When direct PC mode is selected (44 pin PLCC package only), the external glue logic which is used to decode the COM-1 (3F8-3FF), COM-2 (2F8-2FF), COM-3 (3E8-3EF), and COM-4 (2E8-2EF) and select the proper interrupt lines have been implemented within the ST16C650. The ST16C650 provides Three selectable pins to select the desired ports and interrupts for automatic configurations. In addition to these

addresses the ST16C650 decodes two additional addresses for LPT-1 (378-37F, printer port-1), and LPT-2 (278-27F, printer port-2) via OP2 and Baudout pins. These address decodes are used for IBM PC or compatible computers serial and parallel ports. During Direct connect mode all three interrupts functions are three state interrupts, to activate the interrupts MCR bit-3 should be set to "1".

FUNCTIONAL DESCRIPTIONS

The 32 bytes data FIFO's are enabled when user writes to the ST16C550/ST16C650 FIFO control register. With standard 16C550 parts, the user can only set receive trigger levels but not transmit trigger level. The ST16C650 provides independent trigger levels for both receiver and transmitter. To be compatible with ST16C550, 16 bytes transmit trigger level is selected after reset. Note that user can write to transmit trigger levels but activation will not take place till ST16C650 special mode is selected (EFR bit-4 is set to "1"). The ST16C650 is designed to work with high speed modems and shared network environments, that requires fast processing time. By increasing number of characters in the FIFO, networking units can handle more data within same time. Example: ST16C550 with 16 bytes of data, 115.2k and 8 bits wide word and one stop bit, will take 1.52 ms to transmit 16 bytes of data. But with 32 bytes of data buffer it will take 3.05 ms. This will gives additional time for the CPU to process other applications and reduce the interrupt servicing time.

The contents of the Xon-1,2 and Xoff 1,2 are not reset to any given values and user can write any values desired for software flow controls. Different conditions can be set to detect Xon/Xoff characters or start/stop the transmissions. See the table for all possible conditions. When single Xon/Xoff characters are selected, ST16C650 compares the incoming data with these values and controls the transmission, these characters are not stacked in data buffer or FIFO. Special case is provided to detect the special character and stack it into the data buffer or FIFO. These conditions are selected via Enhanced Feature Register (EFR bit 0-3).

Hardware flow control can be selected when either or both bits of the EFR bit 6-7 are set to "1". When auto CTS is selected, the ST16C650 will stop the transmission as soon as a complete character is transmitted and CTS input level is high. Transmission is resumed after CTS input changes to low level.

RTS pin will be forced to high state regardless of it's original state when receive FIFO reaches to the programmed trigger level. RTS pin resumes it original state after content of the data buffer (FIFO) drops below the programmed trigger level. Both hardware and software flow controls can be enabled for automatic operation. During these conditions the ST16C650 will accept additional data to fill the unused transmit and receive FIFO locations.

Special interrupt modes have been added to monitor the hardware and software flow conditions. These are the IER bits 5-7.

The ST16C650 is designed to operate with low power consumption, special sleep mode has been added to stop the clock and reduce the power consumption when it is not used (Green PC). When EFR bit-4 and IER bit-4 are enabled (set to "1"), the ST16C650 enters into sleep mode and resumes it's normal operation when a data is received or state of the modem input pins changes or it is set to transmit data. The ST16C650 stays in this mode till it is disabled.

Special care should be considered for the following interrupt conditions and handling them. After reset if transmitter interrupt is enabled, ST16C650 will issue an interrupt to indicate that transmit holding register is empty, no other interrupts will be issued after enabling the interrupt. The LSR register has highest interrupt priority and CTS, RTS have lowest interrupt priority. The interrupt status register will show the highest interrupt priority condition, and after servicing the interrupt condition next priority interrupt level will be shown. There are two interrupt conditions that have same priority and it is important to know the conditions to service. Receive data ready and receive time out share the same priority with one additional bit (IER bit-3). Receiver issues interrupt after number of characters are reached the programmed trigger level, in this

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case the ST16C650 FIFO holds equal or more characters than the trigger level. After reading block of data, user can check the LSR bit-0 for additional characters. If number of characters in the receive data register did not reach to programmed trigger level within certain time frame, ST16C650 will issue receive data ready interrupt with ISR bit-3 set to "1".

Note that, receive time out is functional only in ST16C550/650 mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be: $T = 4 \times 7$ (programmed word length) +12 = 40 bits Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:

T = 4 X 7(programmed word length) + 12 = 40 bits

Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

Due to number of active simultaneous interrupt limitations in PC and compatibles, ST16C650 offers share interrupt out by setting MCR bit-5 to "1". If this mode is selected, it is required to connect 200-500 ohm resistor between the INTA pin to Ground. Note that other interrupts (INTB, INTC) will be inactive during this mode.

Dual baud rate generator is provided to maintain the 16C550 compatibility and provide higher data rate when it is needed. Example 14.4k to 19.2k modems requires to have 57k to 115.2k data rate and 28.8k modem requiems to have 230.4K. The 16C550 compatible parts can only offer 115.2k to maintain the software compatibility. The ST16C650 utilizes 7.32 MHz crystal/clock and provide 16C550 compatible data rate and higher. ST16C550 and ST16C650 baud

rate generator tables can be selected is setting and resetting the MCR bit-7.

The ST16C650 transmit trigger level, provides additional flexibility to the user for block mode operation. In ST16C550/650 mode LSR bits 5-6 gives indication that transmitter is empty or not, but there is no mechanism to identify FIFO full state or available empty locations in FIFO. User can select one of the two possible ways to operate the transmit and receive FIFO by utilizing the DMA mode (FCR bit-3). When FIFO's are enabled and DMA mode "0" is selected, the ST16C650 sets the interrupt bit and activates interrupt output pin for single transmit and receive operation like ST16C450 mode except it can receive and transmit 32 bytes of characters. When DMA mode "1" is activated, user takes the advantage of the block mode operation. In this mode, transmitter/receiver sets the interrupt flag and interrupt output pin, when characters in the FIFO are below the transmit trigger level or over receive trigger level. Note that since ST16C550 does not have transmit trigger levels, the default trigger level in the ST16C650 is set to 16 bytes (trigger level

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	ready in string appropriate in	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1 1	1	mechanism to identify i	Line Control Register
1 100	0	0	O-Har III emply locations in min-C	Modem Control Register
1	0	11 914 916	Line Status Register	FIFO is empty. The time out court
1	1	0	Modem Status Register	
1	s el jurs d'activat	oor and to	Scratchpad Register	Scratchpad Register
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	80 1 9	MSB of Divisor Latch	MSB of Divisor Latch
0	1	0	Enhanced Feature Register	Enhanced Feature Register
1	0	0	Xon-1 Word	Xon-1 Word
1	0	1	Xon-2 Word	Xon-2 Word
1	1	0	Xoff-1 Word	Xoff-1 Word
1	1	1	Xoff-2 Word	Xoff-2 Word

These registers are accessible only when LCR bit-7 is set to "1". Enhanced Feature Register is accessible only when LCR is set to "FF"

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ST16C650 ACCESSIBLE REGISTERS

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	deldier 91	0/ CTS interrupt	0/ RTS interrupt	0/ Xoff interrupt	0/ Sleep mode	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0/TX trigger (MSB)	0/TX trigger (LSB)	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0 ms, harios	ISR eldamys s	0/ FIFO's enabled	0/ FIFO's enabled	0/ RTS, CTS	0/ Xoff	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop	word length bit-1	word length bit-0
1 0 0	MCR	Clock	0/ IRRT enable	INTA type select	loop back	OP2*/ IRQx enable	OP1*	RTS*	DTR*
1 0 1	LSR 3	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS timener	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8
0 1 0	EFR vile	Auto CTS	Auto RTS	Special Char. select	Enable IER Bits 4-7, ISR, FCR Bits 4-5, MCR Bits 5,7	Cont-3 Tx,Rx Control	Cont-2 Tx,Rx Control	Cont-1 Tx,Rx Control	Cont-C Tx,Rx Contro

These registers are accessible only when LCR bit-7 is set to "1". Enhanced Feature Register is accessible only when LCR is set to "FF"

REGISTER FUNCTIONAL DESCRIPTIONS

OPERATING MODE.

The ST16C650 provides pin selectable interface for existing 16C550 and new designs.

PC mode can be selected by tying the SEL pin to GND. When PC mode is selected the ST16C650 eliminates the external address decode logic (glue logic) for COM1-4 and jumper setting for IRQ3, IRQ4 or IRQn. The ST16C650 can be configured as follows:

S3 S2 S1	Address	ComPort	IRQ
0 0 0	3F8-3FF	COM-1	IRQB**
0 0 1	2F8-2FF	COM-2	IRQC**
0 1 0	3E8-3EF	COM-3	IRQB**
0 1 1	2E8-2EF	COM-4	IRQC**
1 0 0	3F8-3FF	COM-1	IRQA**
1 0 1	2F8-2FF	COM-2	IRQA**
1 1 0	3E8-3EF	COM-3	IRQA**
1 1 1	2E8-2EF	COM-4	IRQA**

^{**} All interrupt outputs are inactive (three state mode) except the selected address.

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going

noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

- A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.
- B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.
- C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C650 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

- A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.
- B) LSR BIT4-1 will specify which error(s) has occurred.
- C) LSR BIT-5 will indicate when the transmit FIFO is empty.
- D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.
- E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C650 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2¹⁶-1. The output frequency of the Baud-out* is equal to 16X of transmission baud rate (Baud-out*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

BAUD RATE GENERATOR PROGRAMMING TABLE (7.372 MHz CLOCK):

BAUD RATE MCR BIT-7=1	BAUD RATE MCR Bit-7=0	16 x CLOCK DIVISOR "Decimal"
50	200	2304
75	300	1536
150	600	768
300	1200	384
600	2400	192
1200	4800	96
2400	9600	48
4800	19.2K	24
7200	28.8K	16
9600	38.4k	12
19.2K	76.8k	6
38.4K	153.6k	3
57.6K	230.4k	2 (
115.2K	460.8k	egistet Empry

HARDWARE FLOW CONTROL OPERATION.

When hardware flow control operation is enabled, the ST16C650 monitors the CTS* pin for transmit operation and receiver trigger level for RTS* operation. When CTS* changes state from low to high, the ST16C650 suspends the transmission operation as soon as complete character is transmitted. ISR bit-5 will be set (if enabled via IER bit 6-7). Transmission will resume as soon as CTS* pin goes low. RTS* pin will be forced to high state when receiver FIFO

reached to the programmed trigger level. RTS* will go low when Receive Holding Register is below next lower trigger level. The ST16C650 will accept additional data when transmission is suspended during hardware flow control till all locations are filled.

SOFTWARE FLOW CONTROL A beidealb a little

When software flow control operation is enabled, the ST16C650 will compare the two sequential receive data with Xoff-1,2 programmed characters. When these characters matched correctly, the ST16C650 will halt the transmission after finishing the transmission of the complete character. The receive ready, Xoff (if enabled via IER bit-5) flags will be set and the interrupt output pin (if receive interrupt is enabled) will be activated. After the recognition of the Xoff characters the ST16C650 will compare next two incoming characters with Xon-1,2 characters. The ST16C650 will resume the operation and clear the flags (ISR bit-4) when Xon characters are received. The ST16C650 will send Xoff-1,2 characters as soon as received data passed the programmed trigger level. The ST16C650 will transmit programmed Xon-1,2 characters as soon as receive data reached to the next lower trigger level.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:

0= disable the receiver ready interrupt. 1=enable the receiver ready interrupt.

IER BIT-1:

0= disable the transmitter empty interrupt. 1= enable the transmitter empty interrupt.

IER BIT-2:

0= disable the receiver line status interrupt. 1= enable the receiver line status interrupt.

IER BIT-3:

0= disable the modem status register interrupt.

a

1= enable the modern status register interrupt.

lower trigger level. The ST16C650 will ac. 4-TIB RBI

0= disable sleep mode. olas manest nertwisted lanoit

1= enable sleep mode. The ST16C650 enters into power down mode and external clock or oscillator ciruit is disabled. Any change of state on the RX, RI*, CTS*, DSR*, and CD* pins start the ST16C650. The ST16C650 will not lose the programmed bits when sleep mode is activated or deactivated. The ST16C650 will not enter in sleep mode if any interrupt these characters matched correctly, the Spribned si

sion of the complete character. The rece:5-TIB/BIT-5:

0= disable the received Xoff interrupt.

1= enable the received Xoff interrupt. The ST16C650 issues an interrupt when Xoff characters are received and correctly matched with Xoff 1,2 words.

will resume the operation and clear the flac:6-TIB RBI

0= disable the RTS interrupt, and be sed on a new (a

Priority level

D5 D4 D3 D2 D1 D0 Source of the interrupt 0 0 1 0 1 0 LSR (Receiver Line Status Register) 2 0 0 0 0 0 RXRDY (Received Data Ready) 1 2 0 0 1 0 0 RXRDY (Receive Data time out) 3 0 0 0 0 0 1 TXRDY(Transmitter Holding Register Empty) 480.8k 0 MSR (Modern Status Register) 4 0 0 0 0 5 0 1 0 0 0 0 RXRDY (Received Xoff signal)/ Special character 6 1 0 0 0 0 0 CTS, RTS change of state HARDWARE FLOW CONTROL

1= enable the RTS interrupt. The ST16C650 issues interrupt when RTS pin changes state from low to high.

Generator that is capable of taking any cit-TIB Rail

0= disable the CTS interrupt. Ib box x M AS-OG mon

1= enable the CTS interrupt. The ST16C650 issues interrupt when CTS pin changes state from low to high.

INTERRUPT STATUS REGISTER (ISR) to 82.1 bos

The ST16C650 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C650 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

76.8

153.6

239.4

The number of stop bits can be specified :0-TIB RSI

0= an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

1= no interrupt pending.

ISR BIT 1-3:

Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-5:

These bits are enabled when FER bit-1 is set to "1". ISR bit-4 indicates that matching Xoff characters have been detected. ISR bit-5 indicates that CTS, RTS have been received or issued. Note that the ISR bit-4 will stay "1" till Xon characters are recieved.

ISR BIT 6-7: 998 4-TIE ROLL beldens at tid yinsq ant II

These bits are not used and are set to zero in ST16C450 mode. BIT 6-7: are set to "1" in ST16C650 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:

0= disable the transmit and receive FIFO.

1= enable the transmit and receive FIFO.

This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:

0= No change. Assid a essuability lid lenthop, Assid

1= Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:

0= No change. do la remoco elar buso lamethi edT

1= Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3: 1 PROPERTY OFFICE

0= No change.

1= Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":

When ST16C650 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":

When ST16C650 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":

When ST16C650 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1": 50 blow and to red

When ST16C650 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the time-out has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:

These bits are used to set the trigger level for the transmit FIFO interrupt. The ST16C650 will issue a transmit empty interrupt when number of characters in FIFO drops below the selected trigger level.

BIT-5	BIT-4	FIFO trigger level
0	0	max that 16 axa an
0	1	8
1	0	24
1	1	30

FCR BIT 6-7: - VOICE Text retained ambient timeners

These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	T. FOR bit	e FIFO mode (FOR bit-0=
0	va.l.	16
1.00	0	24
1	1	28

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:

The number of stop bits can be specified by this bit.

tuon solvis	Stop bit(s)	Word length	BIT-2
moini on =	upi pending.	5,6,7,8	0
SR BIT 1-	1-1/2	5	1
noo Ispino.	ed to 2 tende	6,7,8	ric1 en

LCR BIT-3:

Parity or no parity can be selected via this bit. 0= no parity

1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.

0= ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.

1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.

LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:

Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).

0= normal operating condition.

1= forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:

The internal baud rate counter latch and Enhance Feature mode enable (DLAB).

0= normal operation.

1= Divisor latch and Enhanced Feature register enable.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232). Wal a most beginned

MCR BIT-0:

0= force DTR* output to high. (30 and part selecibril 1= force DTR* output to low. The sortiz state begins to

MCR BIT-1:

0= force RTS* output to high. Of moleculups at the aid T 1= force RTS* output to low.

RTS* is used as hardware flow control signal when enabled via EFR bit-6. RTS* goes high when FIFO is reached to the selected trigger level and goes low as soon as content of the receive holding register is below the trigger level. Content of this register changes with state of the hardware flow control, functioons normally when hardware flow control is disabled.

MCR BIT-2; SOM edit ni STICl of Ineleviups ai fid aidT

0= set OP1* output to high. 1= set OP1* output to low.

MCR BIT-3:

0= set OP2* output to high (STD mode). Forces INTx outputs to three state mode during PC mode selection. 1= set OP2* output to low (STD mode). Sets the INTx outputs to active mode during PC mode selection

MCR BIT-4: drot permilment to the complement to the PTIB ROM

0= normal operating mode.

1= enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modern Control Register instead of the four Modem Control inputs. The inter-

MCR BIT-5:

0= Active or three state interrupt output.

1= Open source interrupt output. Required external

resistor from this pin to ground. This mode is provided for share interrupts.

MCR BIT-6: yest tempia Jased a bevieget tex

0= Standard UART receive and transmit input / output. 1= Infrared receive and transmit input / output.

MCR BIT-7:

0= Normal or divide by one clock input. Standard ST16C550 baud rates can be selected when this bit is set to "0" and 1.8432 MHz crystal is used.

1= Divide by four clock input. Standard ST16C550 baud rates can be selected when this bit is set to "1" and 7.372 MHz crystal is used. an artible of impress =0

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU, in one gretation files bee political retilimens of =0

LSR BIT-0: one of the sit is set to one was:0-TIR RL 0= no data in receive holding register or FIFO. 1= data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:me primed none value end tasel to #1 0= no overrun error (normal).

1= overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO. The state of the st

LSR BIT-2: control input from the MODEM changes :-

0= no parity error (normal).

1= parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:

0= no framing error (normal).

1= framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:

0= no break condition (normal).

1= receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:

It indicates that the ST16C650 is ready to accept a new character for transmission. In addition, it causes the ST16C650 to issue an interrupt to the CPU when the transmit holding register empty interrupt enable is set.

0= transmit holding register is not empty.

1= transmit holding register (or FIFO) is empty. CPU can load the next characters. When this bit is set, CPU can load upto 32 bytes of data to the ST16C650.

LSR BIT-6: stab to autata eril sebivoig retaiped zin'i

0= transmitter holding and shift registers are full.
1= transmitter holding and shift registers are empty.
In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:

0= normal.

1= at least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0: ebern CPIP ent ni nedermond viting

Indicates that the CTS* input to the ST16C650 has changed state since the last time it was read.

MSR BIT-1:

Indicates that the DSR* input to the ST16C650 has changed state since the last time it was read.

MSR BIT-2:

Indicates that the RI* input to the ST16C650 has changed from a low to a high state.

MSR BIT-3:

Indicates that the CD* input to the ST16C650 has changed state since the last time it was read.

MSR BIT-4:

This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

CTS* functions as hardware flow control signal input if it is enabled via EFR bit-7. Transmit holding register is gated with this input to start/stop the transmission. A high at this pin will stop the transmission as soon as complete character is transmitted.

MSR BIT-5:

This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:

This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7: eborn 39 graph abom evibe of stugtuo

This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C650 provides a temporary data register to store 8 bits of information for variable use.

ENHANCED FEATURE REGISTER (EFR)

Enhanced Features can be Enable/Disabled via this register.

EFR BIT 0-3:

Combinations of software flow control can be selected by programming this bits.

3

Cont-3	Cont-2	Cont-1	Cont-0	Tx, Rx saftware flow controls	
0	0	X	X	No transmit flow control	MOR
1	0	X	X	Transmit Xon1, Xoff1	
0	1	X	X	Transmit Xon2, Xoff2	
1	1	X	X	Transmit Xon1 and Xon2 : Xoff1, Xoff2	
X	X	0	0	No receive flow control	
X	X	1	0	Receiver compares Xon1, Xoff1	
X	X	0	1	Receiver compares Xon2, Xoff2	
1	0	1	1	Transmit Xon1, Xoff1. Receiver compares Xon1 or Xon2, Xoff1 or Xoff2	
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2	
1	9 7 1	1	1 1 6	Transmi Xon1 and Xon2 : Xoff1 and Xoff2	
	\$ D B D	6 6 9 6		Receiver compares Xon1 and Xon2 : Xoff1 and Xoff2	
0	0	1	10	No transmit flow control Receiver compares Xon1 and Xon2 : Xoff1 and Xoff2	

EFR BIT-4:

Enhanced interrupt control bit.

0= disables the IER bits 4-7 and ISR bits 4-5. Standard ST16C550 mode.

1= enables the enhanced interrupt functions.

EFR BIT-5:

0= Normal.

1= Special character detect. ST16C650 compares the incoming receive data with Xoff-2 data. Up on correct match, the received data will be transferred to FIFO

and ISR Bit-4 will be set to indicate detection of special character.

EFR BIT-6:

RTS* flow control.

0 = Normal. RTS* flow control is disabled. Standard ST16C550 mode.

1 = RTS pin goes high when receive FIFO's are reach to the programmed trigger level.

EFR Bit-7:

CTS* flow control.

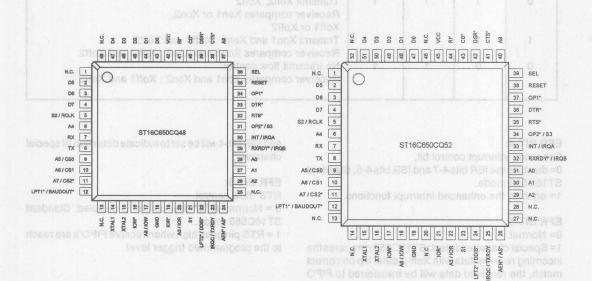
0 = Normal. CTS* flow control mode is disabled. Standard ST16C550 mode.

1 = Transmission is resumed when low input signal is detected on the CTS* pin.

ST16C650 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0 losingo woll
LSR	LSR BITS 0-4=0,
	LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, SnoX bna f
	MSR BITS 4-7= input signals
FCR	FCR BITS 0-7=0 MOX 251891
FER	FER BITS 0-7=0% SnoX eensge

SIGNALS	RESET STATE
TX	High
OP1*	High
OP2*	High
RTS*	High
DTR*	High
RXRDY*	High (STD mode),/ Three state (PC mode)
TXRDY*	High (STD mode) / Three state (PC mode)
IRQn/NT	Low (STD mode) / Three state (PC mode)



AC ELECTRICAL CHARACTERISTICS

 $T_{\Delta}=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
50Q-m3	Cleak high pulse duration	50				actage dissipation
T ₁ T ₂ T ₃ T ₄ T ₅ T ₆ T ₇ T ₈ T ₉	Clock high pulse duration	50 50			ns	External clock
T ²	Clock low pulse duration Clock rise/fall time	50		10	ns	External clock
T ³	Baud out rise/fall time		some	10	ns	100 pF load
T4	Address strobe width	30		100	ns	100 pr load
T 5		30	eiwnertto	unlesc	ns	=0" - 70" C. Vcc=5
T 6	Address setup time Address hold time	5		DOM: NO	113	A STATE OF THE PARTY OF THE PAR
7		5			ns	
T8	Chip select setup time Chip select hold time	0		18068	ns	ladinye
T 9	IOR* to DDIS* delay	U		25		
T ₁₁	Data setup time	15		25	ns	100 pF load Note: 1
T ₁₂	Data hold time	15		18	ns	
T ₁₃		10		191	ns	Note: 1
T ₁₄	IOW* delay from chip select IOW* strobe width	50			ns	Note: 1
T ₁₅	Chip select hold time from IOW*	0			ns	Note: 1
T ₁₆		55	Shuts	atuo lis	ns	Note: 1
T ₁₇ Tw	Write cycle delay	105			ns	iri augiaOV
	Write cycle=T ₁₅ +T ₁₇ Data hold time			25	ns	awaa evA
T ₁₉		15 10		25	ns	printer and
T ₂₁	IOR* delay from chip select IOR* strobe width	65		ment	ns ns	Note: 1
T ₂₃	Chip select hold time from IOR*	0				tant hand I
T ₂₄	Read cycle delay	55	A		ns	Note: 1
T ₂₅ Tr	Read cycle delay Read cycle=T ₂₃ +T ₂₅	115			ns	
	Delay from IOR* to data	113		35	ns ns	100 pF load
T ₂₆	Delay from IOW* to output			50	ns	100 pF load
T ₂₈	Delay to set interrupt from MODEM			70	ns	100 pF load
T ₂₉	Delay to reset interrupt from IOR*			70	ns	100 pF load
T ₃₀	input			70	115	100 pr load
T ₃₁	Delay from stop to set interrupt			1		100 pF load
T ₃₂	Delay from IOR* to reset interrupt		100	1 _{RCIk} 200	ns	100 pF load
T 32	Delay from initial INT reset to transmit	8		24	*	100 pr load
T ₃₃	start	O		24		
T ₃₄	Delay from stop to interrupt		1	100	ns	
T 34	Delay from IOW* to reset interrupt			175	ns	
T ₃₅	Delay from stop to set RxRdy			11	115	
T ₄₅	Delay from IOR* to reset RxRdy			1 _{RCLK}	μS	
T ₄₆	Delay from IOW* to set TxRdy			195	ns	
T ₄₇	Delay from start to reset TxRdy		1	8	*	
47	Dolay Holli Start to 1636t TXINGY			0		

Applicable only when AS* is tied low * = Baud-out* cycle Note 1:

AC ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

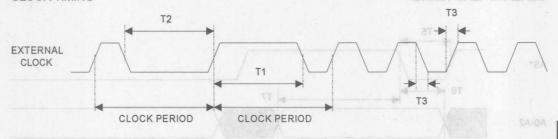
Supply range			7 Volts
Voltage at any pin Operating temperature			GND-0.3 V to VCC+0.3 V 0° C to +70° C
Storage temperature			-40° C to +150° C
Package dissipation			Wm 000 Clock high pulse duration

DC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol		Parameter Limits Min Typ Max		Max	Units	Conditions			
VILCK VIHCK VIL VIH VOL VOH ICC VOP ISLP IIL ICL	Clock input low level Clock input high level Input low level Input high level Output low level on all outputs Output high level Avg power supply current Operating voltage Avg sleep mode current Input leakage Clock leakage			3 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	-0.5 3.0 -0.5 2.2 2.4 2.7	1.2 750	0.6 VCC 0.8 VCC 0.4 5.50 ±10	V V V V MA V ДА ДА ^	In a set of the control of the contr
	100 pF to 100 pF to 100 pF to 100 pF to 100 pF to	an an an an an	35 50 70 70 200 200 24		S sin	n IOR* rupt terrupt to transi	o output out from I rupt from set inter reset in iT reset	n IOR* to n IOW* to et Interruptent eset inter n IOR* to n IOR* to n Initial IN	Delay from Delay from Delay from Delay to s input Delay from Delay from Delay from Delay from Delay from Start
		en en en *	100 175 176 195 195					n IOW" in stop to in IOR" to	Delay from Delay from Delay from Delay from Delay from Delay from

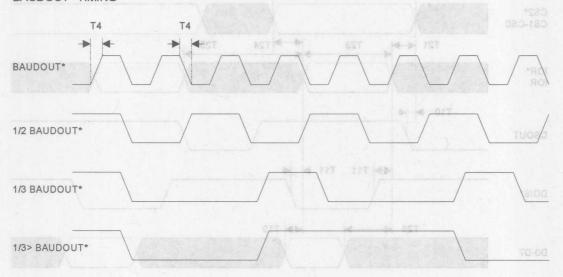
CLOCK TIMING

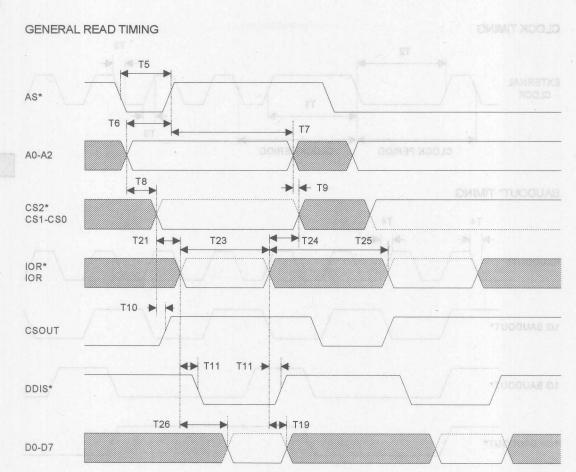


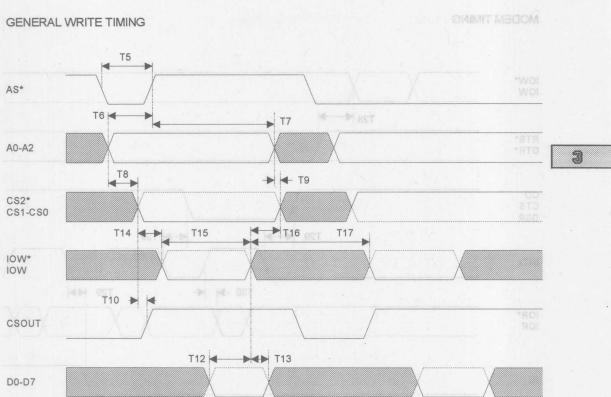
et by be

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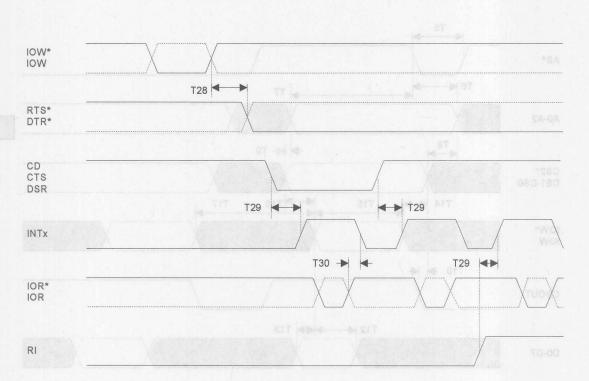
BAUDOUT* TIMING

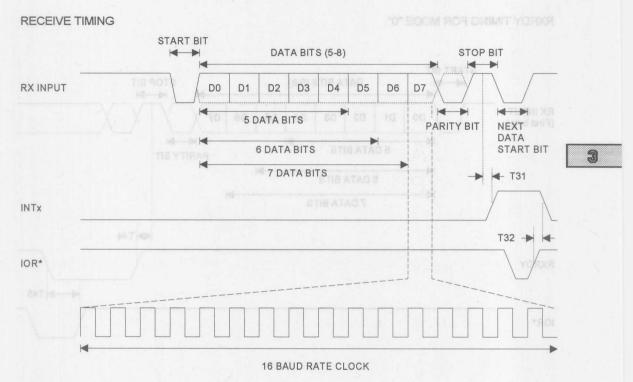




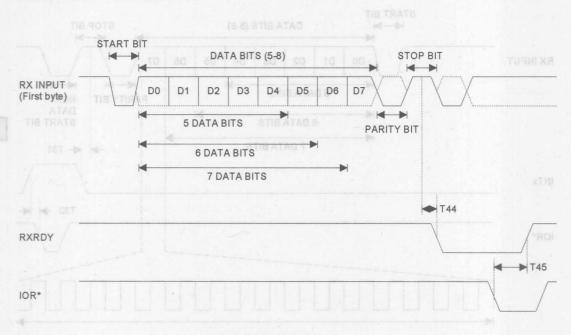




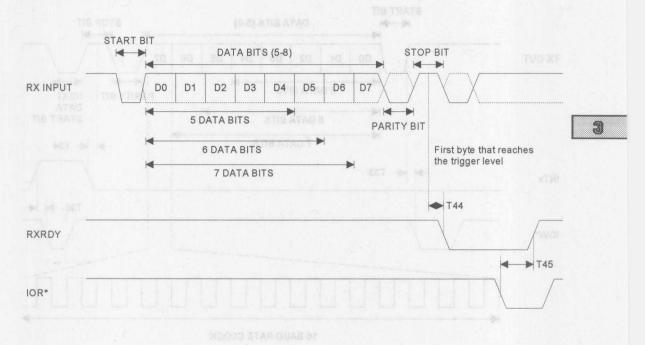


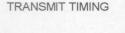


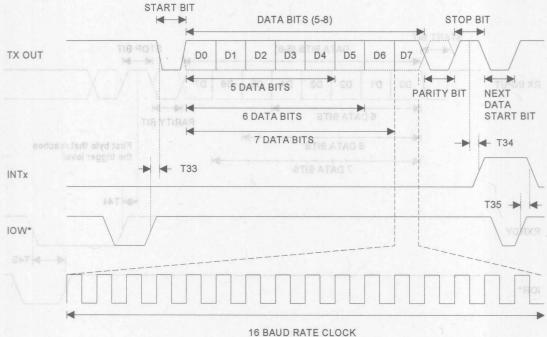
RXRDY TIMING FOR MODE "0"



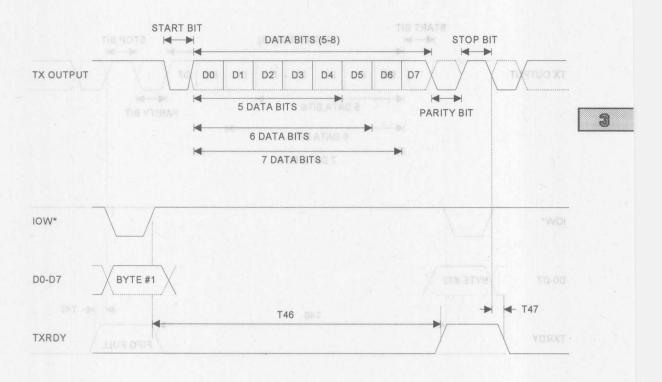
RXRDY TIMING FOR MODE "1"



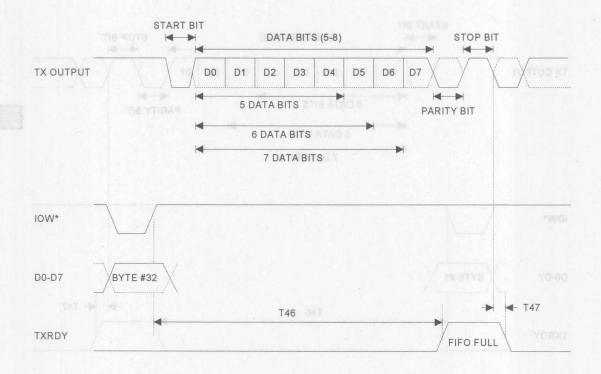




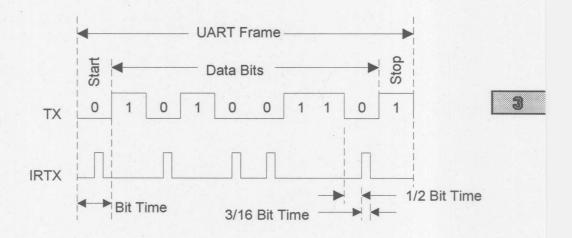
TXRDY TIMING FOR MODE "0"

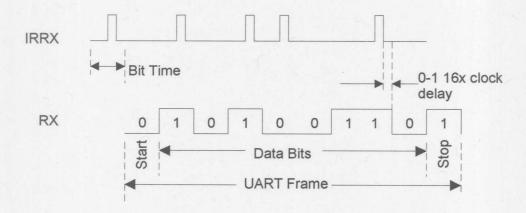


TXRDY TIMING FOR MODE "1"

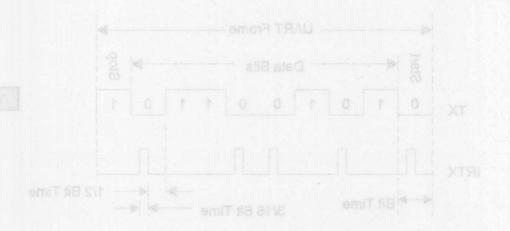


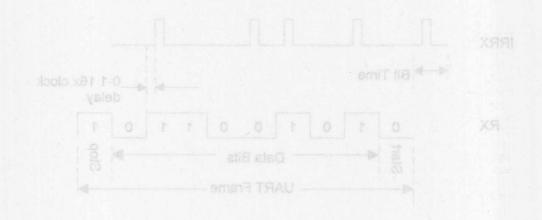
IR TRANSMIT AND RECEICE INPUT/OUTPUT TIMING





IR TRANSMIT AND RECEICE INPUT/OUTPUT TIMING







Printed September 8, 1994

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH PARALLEL PRINTER PORT

DESCRIPTION

The ST16C452 is a dual universal asynchronous receiver and transmitter with a bi-directional CENTRONICS type parallel printer port. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

STARTECH ST16C452PS provides additional features to control the printer port direction without any additional external logic.

The ST16C452 is an improved version of the VL16C452 UART with higher operating speed and lower access time. The ST16C452 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C452 provides internal loop-back capability for on board diagnostic testing.

The ST16C452 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

FEATURES

- Pin to pin and functional compatible to VL16C452, WD16C452
- Fully compatible with all new bi-directional PS/2 printer port registers.
- Modern control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Independent transmit and receive control
- Software compatible with INS8250, NS16C450
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source.
- · Bi-directional hardware/software parallel port
- · Bi-directional I/O ports

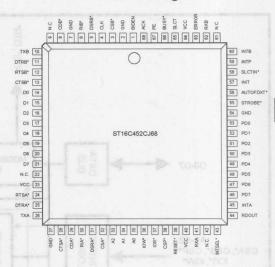
ORDERING INFORMATION

 Part number
 Package
 Operating temperature

 ST16C452CJ68
 PLCC
 0° C to + 70° C

 ST16C452IJ68
 PLCC
 -40° C to + 85° C

PLCC Package

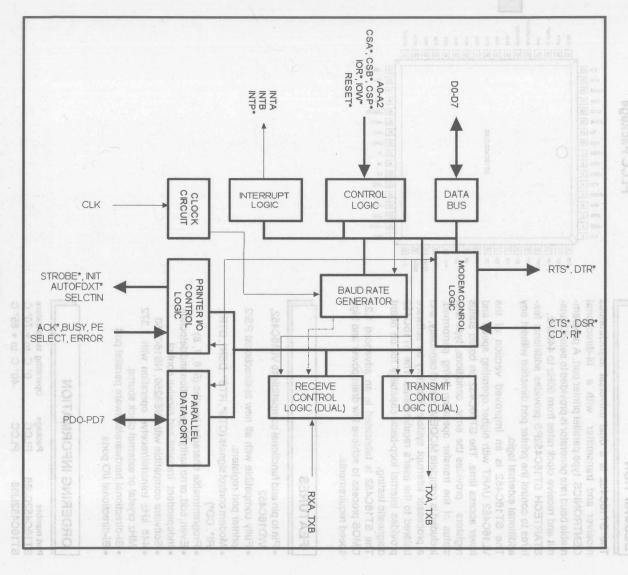


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S 1 16 C 45 2 P S

JELJASIAS HTM

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
		ng, OVI ot A/I3 (active to a) as been detected	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
		sift SVA Jugius	Address select lines. To select internal registers.
CLK	t jezer 4 jnhub beldszib ei n	additional start, sta nark (http://stave. han the transmite	Clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
(MCR bit-0). output to low: a "0" to that	we de t e. Thi ontrol register ill setthe DTR de after willing	is ready A/B (Jo is read) to reserve for the modern or atthe MICR bit-Cw be set to high sta	Printer direction select. A high puts the parallel port in the input mode for ST16C452AT and software controlled mode (input/output) to ST16C452PS. Allow sets the ST16C452 to output mode.
IOW*	36	fter the resot. Not in the (r l insmill et r send A/B réclive	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR* of magain	gnimi 37 nee htes iliw (†-ild	send was (adired that daily seat (MCR) the meet this pile	Read strobe (active low). A low level on this pin transfers the contents of the ST16C452 data bus to the CPU.
RDOUT	encat 6 44 to 10	not h Ot any e fo	Read select out (active high). This pin goes high when the CPU is reading data from the ST16C452 to en/disable the external transceiver or logic's.
RESET*	as algolal (wol)	nput AJE. The self- oort to streeck51 come and a space ok mode the RX in	Master reset. (active low) A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CS A/B*	32,3	and connected to I I nd A/B (active In	Chip select A/B (active low). A low at this pin enables the serial port-A/B / CPU data transfer operation.
DSR A/B*	(dgal sylba a)	otrol function life ading the MSR E T costive operation gut A/B (three sta	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
RI A/B*	30,6	enabled by the inte iver enrin, receive edem stehns cond	

3

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
	on the CPU. DO		
	29,8 000		
	of beau of no. and more and more and no.	An external cloc	Serial data output A/B. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
	pt puls the pare le and software cont and software cont S. Allow sets the S ow on this pin will be to the addresses	or ST16C452AT U to ST16C452B L (active low), A	Data terminal ready A/B (active low). To indicate that ST16C452 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
*AVA STR in transfers CPU.	24,12 Q aid in a level wo state of the book work of the book of the book work of the book w	O (active low), A out (active high	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
	41,62 Illwing alltino wo resturance of T e len ganub belds	I (active low) A I internal register r input will be dia	Serial data input A/B. The serial information (data) received from serial port to ST16C452 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
CTS A/B*		/B / CPU data ta dy A/B (active lo lis ready to exch	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
INT A/B	45,60	O BIA natioibni	Interrupt output A/B (three state active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.

SYMBOL DESCRIPTION

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
aut pin, When	iks the ACK* in	rupt ou'put (actinont. This pin train INTE ON wand w	enables the parallel port / CPU data transfer operation.
		ect mode. The e	during output mode.
STROBE*	nothi 55*az liiv	this piO\t VCC ing the status of VTP output.	General purpose I/O or data strobe output (open drain active low). This output indicates to the printer that valid
AUTOFDXT*	and 56* on it.	bruu(/O rawoo	General purpose I/O or automatic line feed (open drain active low). When this signal is low the printer should automatically line feed after each line is printed.
NITsmemi bei	enno:57* aniq	y inpu o\ III powe	General purpose I/O or initialize line printer (open drain active low). When this signal is low it causes the printer to be initializes.
SLCTIN*	58*	1/0	General purpose I/O or line printer select (open drain active low). When this signal is low it selects the printer.
ERROR*	63*	1	General purpose input or line printer error (active low) This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	65*	I SAV	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	ole Register	Transmit Hol Interrupt Ens	General purpose input or line printer busy (active high). An output from the printer to indicate printer is not ready to accept data.
PE		Line Control I Modem Cont	General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.
ACK*	ir Lateli	Seratoloped F LSB of Divisor MSB of Divisor	General purpose input or line printer acknowledge (active low). This input is pulsed low by the printer to indicate that data has been accepted successfully.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
sensfer data in		ter por O rip sete parallel port / C alparallel port / C alparallel ports (f alparalle	Printer interrupt output (active low). To signal the state of the printer port. This pin tracks the ACK* input pin, When ACK* is low INTP is low and when ACK* is high INTP is high
INTSEL*	43 strobe outp	at model pase I/O or du Trils output ind lable at the print	Interrupt select mode. The external ACK* can be selected as an interrupt source by connecting this pin to the GND. Connecting this pin to VCC will set the interrupt to latched mode, reading the status register of the printer section resets the INTP output.
	self is low the	nose O or au When this sign ly line feed after	Signal and power ground. All ground pins are connected internally.
VCC (1000)	23,40,64	tini 10 du esogi	Power supply input. All power pins are connected internally.

^{*} Have internal pull-up resistor on inputs

PROGRAMMING TABLE FOR SERIAL PORTS A/B

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0 0	nhd ets	output from the printer to indicate	Interrupt Enable Register
0	1	0	Interrupt Status Register	
0	1	1		Line Control Register
iloit) y	0	0	General gurgose inout or line p	Modem Control Register
- 1	0	pibri1 of r	Line Status Register	
1	1	0	Modem Status Register	
1011 8	poshton	os funir	Scratchpad Register	Scratchpad Register
0	0	theOods	low). This input is pulsed low by	LSB of Divisor Latch
0	0	⊿1แล้	data has been accepted success	MSB of Divisor Latch

ST16C452 ACCESSIBLE REGISTERS

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1 dqun iqun	IER e status inter e status inter	0 sceiver lin ceiver lin	IT-20 table the nable the the the the the the the the the th		nsroller register mitter is mit snift be per-	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
-		010	1	nedeon sta	able one of ble the r	0	nptyoflag rinternal x stoold	regioer er ië receive dooks (1)	INT priority bit-1	INT priority bit-0	INT status
0	1	1 (9)	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 ni b	0	0 inon	MCR	0 Sprovides Sminker	0 ST16C45I	0	loop back	INT enable	Not used	RTS*	DTR*
Felippi son son iced	0	t Skal errup the S	LSR of the sort state of the s	ransors. es the sol uring the	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
	1.	0	MSR	CD	RI RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1	1	1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

DLL and DLM are accessible only when LCR bit-7 is set to "1".

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REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C452 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2¹⁶ -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:

0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:

0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:

0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:

0=disable the modem status register interrupt. 1=enable the modem status register interrupt.

IER BIT 7-4:

All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C452 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C452 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

Р	D2	D1	D0	Source of the interrupt
1	1	1	0	LSR (Receiver Line Status
2	1	0	0	Register) RXRDY (Received Data
3	0	1	0	Ready) TXRDY(Transmitter Holding
4	0	0	0	Register Empty) MSR (Modern Status Register)

ISR BIT-0:

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

1=no interrupt pending.

ISR BIT 1-2:

Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:

These bits are not used and are set to "0".

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1(98)	PRETERY
1	0	7
011100	date hf the	rides 8 corrent

LCR BIT-2: " If of the end and about moltemorni

The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	el ed) donie s
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:

Parity or no parity can be selected via this bit.

1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.

0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.

1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5: "GO FREG FETO, (XFI) bugninevisors effi

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.

LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6: at the lower Common mobile and to beaten

Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).

0=normal operating condition.

1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:

The internal baud rate counter latch enable (DLEN). 0=normal operation.

1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:

0=force DTR* output to high.

1=force DTR* output to low.

MCR BIT-1:

0=force RTS* output to high.

MCR BIT-2: wined bevieces set abberto data revieces

This bit is used for internal loop-back mode, and is not used for regular operation.

MCR BIT-3:

0= sets the INT output pin to three state mode.
1= enables the INT output pin.

MCR BIT-4: priorof yd beterenep ai tid ythag MEVE =1

0=normal operating mode.

1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2,3are connected to modem control inputs. In this mode, the receiver and transmitter interrupts

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7; or OCT hadron retrimental edit secret=1

Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR) build is main and

This register provides the status of data transfer to CPU.

LSR BIT-0:

0=no data in receive holding register and saved in the receive holding register.

LSR BIT-1:

0=no overrun error (normal).

1=overrun error, next character arrived before receive holding register was emptied.

LSR BIT-2:

0=no parity error (normal)...s nothing all quantities =0

1=parity error, received data does not have correct parity information.

LSR BIT-3:

0=no framing error (normal).

1=framing error received, received data did not have a valid stop bit. In

LSR BIT-4:

0=no break condition (normal).

1=receiver received a break signal (RX was low for one character time frame).

LSR BIT-5:

0=transmit holding register is full. ST16C452 will not accept any data for transmission.

1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:

0=transmitter holding and shift registers are full. 1=transmitter holding and shift registers are empty.

LSR BIT-7:

Not used. Set to "0".

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0: Partie got a strong thow the series

Indicates that the CTS* input to the ST16C452 has changed state since the last time it was read.

MSR BIT-1:

Indicates that the DSR* input to the ST16C452 has changed state since the last time it was read.

MSR BIT-2:

Indicates that the RI* input to the ST16C452 has changed from a low to a high state.

MSR BIT-3:

Indicates that the CD* input to the ST16C452 has changed state since the last time it was read.

MSR BIT-4:

This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:

This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:

This bit is equivalent to MCR bit-2 during local loopback mode. It is the compliment of the RI* input.

MSR BIT-7:

This bit is equivalent to MCR bit-3 during local loopback mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C452 provides a temporary data register to store 8 bits of information for variable use.

SIGNAL	RESET STATE
TX	High
RTS*	High
DTR*	High
INT	Three state mode

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

E	BAUD RATE	16 x CLOCK DIVISOR	% ERROR
	50	2304	0
1	75	1536	-
1	110	1047	0.026
150	134.5	857	0.058
	150	768	
	300	384	
7	600	192	ARALLEL POR
	1200	96	
-	2400	48	
918	3600	32	KIRCHONITS
	4800	24	
	7200	16	STISCHBAAT
0	9600	12	ST180452PS
	19.2K	6	ST16C452PS
	38.4K	X 3	ST180452AT
1	56K	2	2.77
1	115.2K	1 1	STIBOASSPS

ST16C452 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	BITS 0-7=0
ISR	BIT-0=1, ISR BITS 1-7=0
LCR	BITS 0-7=0
MCR	BITS 0-7=0
LSR	BITS 0-4=0.
	LSR BITS 5-6=1 LSR, BIT 7=0
MSR	BITS 0-3=0,
	MSR BITS 4-7=input signals

3

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW*	IOR*
RORR	0	PORT REGISTER	PORT REGISTER
0	1	I/O SELECT REGISTER	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER

* Reading the status register will reset the INTP output. Isool group ROM and it RTS of the styling at the LINTP output.

PARALLEL PORT DIRECTION SELECT REGISTER (WRITE ONLY)

ST16C452XX	CONTROL	REGIS	TER (D5)	BIDEN	I/O SELECT REGISTER	PORT DIRECTION
ST16C452AT	24	X	7200	0	X	Output mode
ST16C452PS	12	X	0088	0	AA Hex	Input mode
ST16C452PS	0	X	19.2K	0	0001 400 (55 Hex Salid 90)	Output mode
ST16C452AT	3	X	38.4K	. 1	himent of thXRI* input.	Input mode
ST16C452PS	\$	0	SBK	1	X	Output mode
ST16C452PS		1	115.2K	1	X	Input mode

STABOASS EXTERNAL RESET CONDITION

RESET STATE		
BITS 0-7=0 BIT-0=1, ISR BITS 1-7=0 BITS 0-7=0 BITS 0-4=0, BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0	JER ISR LOR MOR LSR	
BITS 0-3±0, MSR BITS 4-7=input signals		

Note: Whenever MSR 8IT3-0; is set to logic "1", NODEM Status interrupt is generated.

loop-back mode, it is the compliment of the CTS*

SCRATCHPAD REGISTER (SR)

ST18C452 provides a temporary data register to store
8 bits, of information for yadable use

TATE	RESETS	
		XT
		P STO
e mode		TIME

PRINTER PORTREGISTER DESCRIPTIONS

PORT REGISTER

Bi-directional printer port. 7 JAVRATXA SANDANTA

Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports. Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:

PD7-PD0 bi-directional I/O ports.

STATUS REGISTER

This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:

Not used. Are set to "1" permanently.

SR BIT-2:

Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK*
input.

1= no interrupt is pending

Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:

ERROR* input state.
0= ERROR* input is in low state
1= ERROR* input is in high state

SR BIT-4:

SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:

PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:

ACK* input state.

0= ACK* input is in low state

1= ACK* input is in high state

SR BIT-7:

BUSY input state.

0= BUSY input is in high state at Judan \$250,718 = 0

1= BUSY input is in low state at Judan \$250,718 = 0

COMMAND REGISTER Tournes Jugue TXCFOTUA

The state of the STROBE*, AUTOFDXT*, INIT, SLCTIN* pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:

STROBE* input pin. Selected field of the elifected TIMI =1 0= STROBE* pin is in high state 1= STROBE* pin is in low state

COM BIT-1: etata ripid of les al huqtuo *I/ITOJI2 =0

AUTOFDXT* input pin. of the state of AUTOFDXT* pin is in high state of AUTOFDXT* pin is in low state

COM BIT-2:

INIT input pin.

0= INIT pin is in low state

1= INIT pin is in high state

1= INIT pin is in high state

1= INIT pin is in high state

COM BIT-3:

SLCTIN* input pin.

0= SLCTIN* pin is in high state

1= SLCTIN* pin is in low state

COM BIT-4:

Interrupt mask.
0= Interrupt (INTP output) is disabled
1= Interrupt (INTP output) is enabled

COM BIT 7-5:

Not used. Are set to "1" permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE*, AUTOFDXT*, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:

STROBE* output control bit.

0= STROBE* output is set to high state

1= STROBE* output is set to low state

CON BIT-1:

AUTOFDXT* output control bit.
0= AUTOFDXT* output is set to high state
1= AUTOFDXT* output is set to low state

CON BIT-2: perits Ou and to assimages resigns sint.

INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:

SLCTIN* output control bit.
0= SLCTIN* output is set to high state
1= SLCTIN* output is set to low state

CON BIT-4:

Interrupt output control bit. 0= INTP output is disabled 1= INTP output is enabled

CON BIT-5:

I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.

0= PD7-PD0 are set for output mode

1= PD7-PD0 are set for input mode

CON BIT 7-6:

Not used.

I/O SELECT REGISTER : (Jumpso 977kl) journalmi at

Software controlled I/O select.

Bi-directional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one"

Hardware/software I/O select.

Bi-directional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or "55" Hex for output. I/O select register and control register bit-5 are only available for ST16C452PS parts.

ST16C452 EXTERNAL RESET CONDITION

SIGNALS	RESET STATE	
PD0-PD7 STROBE* AUTOFDXT*	low, output mode High, output mode High, output mode	states (
INIT SLCTIN*	Low, output mode	

ST16C452 PRINTER PORT REGISTER CONFIGURATIONS

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
	REGISTER	en (READ O				ck few pulse ock rise/fall tin p select setur p select hold	T _s Clo
D7	D6	D5	D4	D3	D2	D1	D0
BUSY*	ACK	PE	SLCT OF	ERROR STATE		v delay min N* delay 1 man N* strobe wid	
		en en	55 55 105			rrupt ot (PS only)	
COMMAN	ID REGISTER	R (READ O	NLY) 68			a noid time ?" delay from ?" strobe widt	
D7	D6	D5	D4	D3	D2	D1.	D0
	100 pF tos	20 ns		SLCTIN*	INIT so of tugino of *	AUTO- FDXT*	STROBE*
	100 pF los 100 pF los 100 pF los 100 pF los	70 ns ns ns ns ns ns ns 24 ns 24 ns	1= IRQ enabled	OR* ot rupt	terrupt from it to set interrup to reset inter	lay to reset in lay from stop lay from IOR* lay from Initia	inp T _{sc} Del T _{sc} Del
CONTRO	L REGISTER	(WRITE	ONLY)				
D7	D6	D5	D4	D3	D2	D1	D0
	-	I/O SELECT	IRQ MASK	SLCTIN*	INIT	AUTO- FDXT*	STROBE*
	0=Output	(PS only)	0=INTP o	utput		7 55 Tar	

AC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
- 00	D3 PD2 PD1	50			PD5	609 70
- 1	Clock high pulse duration	50			ns	
T ₁ T ₂ T ₃ T ₈ T ₉ T ₁₁	Clock low pulse duration Clock rise/fall time	50		40	ns	External clock
13		-		10	ns	
T8	Chip select setup time	5	74		ns	STATUS REGISTER
<u>_</u> 9	Chip select hold time	U	1.5		ns	
_11 /	IOR* to DDIS* delay	145	10	25	ns	100 pF load
T ₁₂	Data set up time	15	1		ns	5ti 1t
T ₁₃	IOW* delay from chip select	10	SLOT		ns	1271.0
T ₁₄	IOW* delay from chip select	10	-1070		ns	IUSY* ACK
T ₁₅ T ₁₆	IOW* strobe width	50			ns	
T ₁₆	Chip select hold time from IOW*	0			ns	
T ₁₇	Write cycle delay	55			ns	
Tw	Write cycle=T ₁₅ +T ₁₇	105	0.11		ns	
T ₁₉	Data hold time	15			ns	
T ₂₁ T ₂₃ T ₂₄	IOR* delay from chip select	10			ns	
T ₂₃	IOR* strobe width	65	(x		ns	OMMAND REGISTE
T ₂₄	Chip select hold time from IOR*	0			ns	
T ₂₅	Read cycle delay	55	104		ns	90 30
Tr	Read cycle=T ₂₃ +T ₂₅	115			ns	
T ₂₆	Delay from IOR* to data		ORI	35	ns	100 pF load
T ₂₈	Delay from IOW* to output		ENABL	50	ns	100 pF load
T ₂₈ T ₂₉	Delay to set interrupt from MODEM			70	ns	100 pF load
20	input		0.081 =0			
T ₃₀	Delay to reset interrupt from IOR*		dist	70	ns	100 pF load
T ₃₀ T ₃₁ T ₃₂	Delay from stop to set interrupt		1= IRQ	1 _{CLK}	ns	100 pF load
T.,	Delay from IOR* to reset interrupt		ene .	200	ns	100 pF load
T ₃₃	Delay from initial INT reset to transmit start	8		24	*	

AUTO- FDXT*			

AC ELECTRICAL CHARACTERISTICS

 $T_A = 0^{\circ} - 70^{\circ}$ C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min Typ Max			Units	Con	ditions
T ₃₄ T ₃₅ T ₃₉ T ₄₀ T ₄₁ T ₄₂ T ₄₃	Delay from stop to interrupt Delay from IOW* to reset interrupt ACK* pulse width PD7-PD0 setup time PD7-PD0 hold time	75 10 25	STICS	100 175	ns ns ns ns		
T ₄₂ T ₄₃	Delay from ACK* low to interrupt low Delay from IOR* to reset interrupt	5 5		19300	ns ns		
N	Baud rate devisor	1		216-1	ut low lev	Ciock ins	

Vent input level to the level t

ABSOLUTE MAXIMUM RATINGS

Supply range
Voltage at any pin
Operating temperature
Storage temperature
Package dissipation

7 Volts
Defliceds estimated assign & 01 = GND-0.3 V to VCC+0.3 V
0° C to +70° C
-40° C to +150° C

500 mW

DC ELECTRICAL CHARACTERISTICS

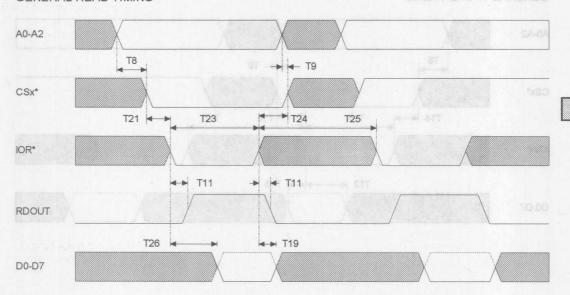
 $T_A = 0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
V _{ILCK}	Clock input low level	-0.5 3.0		0.6 VCC	devisor	N Baud rate
VIHCK VIL VIH	Input low level Input high level	-0.5 2.2		0.8 VCC		Vote 1 * = Baudo
V _{oL}	Output low level			0.4	V	$I_{ol} = 6.0 \text{ mA D7-D0}$ $I_{ol} = 20.0 \text{ mA PD7-PD0}$ $I_{ol} = 10 \text{ mA}$ $SLCTIN*,$ $INIT*,STROBE*,$ $AUTOFDXT*$ $I_{ol} = 6.0 \text{ mA on all}$ other outputs
V _{OH}	Output high level	2.4			V	I_{OH} = -6.0 mA D7-D0 I_{OH} = -12.0 mA PD7-PD0 I_{OH} = -0.2 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OH} = -6.0 mA on all the outputs
I _{CC} I _{IL} I _{CL} RIN	Avg. power supply current Input leakage Clock leakage Internal pull-up resistance	4	12	±10 ±10 15	mA μA μA kΩ	* Marked pins

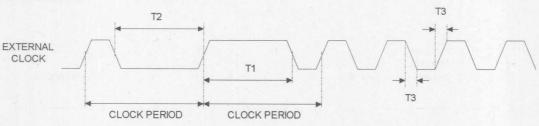
ST16C452AT/PS

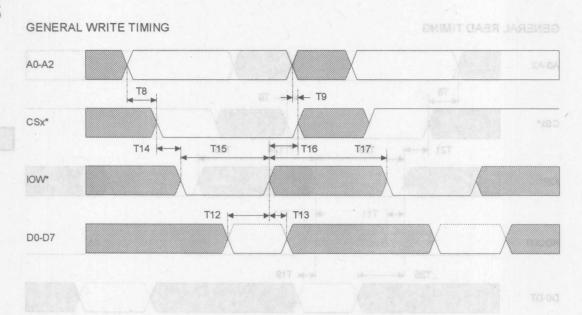
3

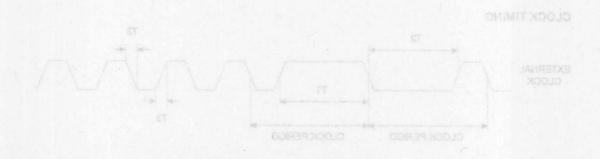
GENERAL READ TIMING



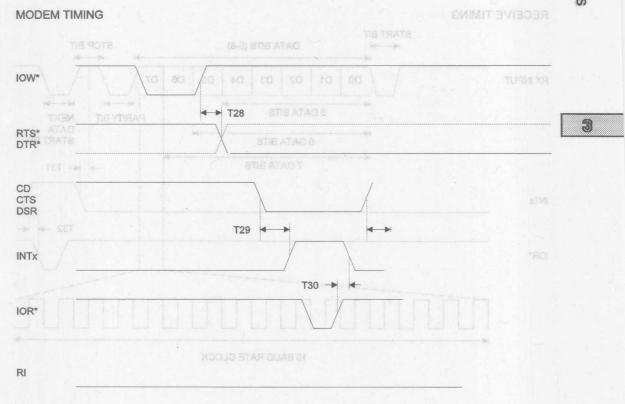
CLOCK TIMING

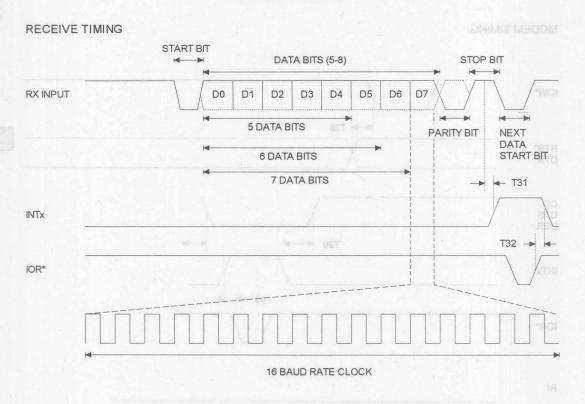




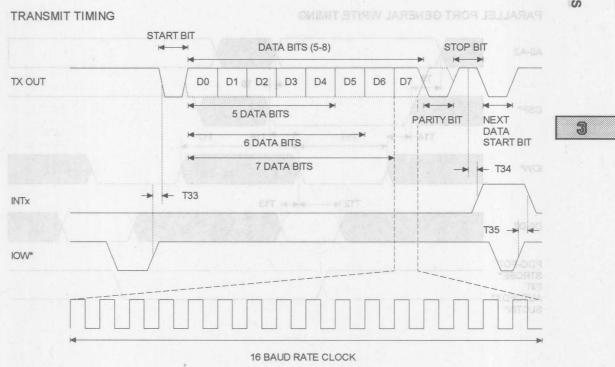


ST16C452AT/PS

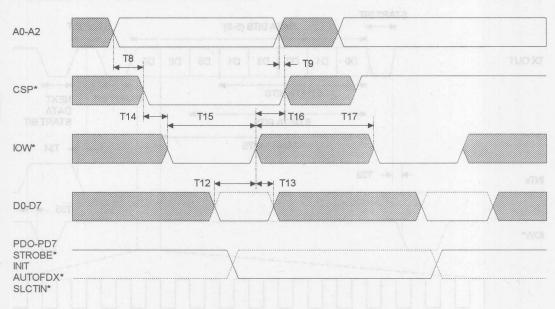




ST16C452AT/PS

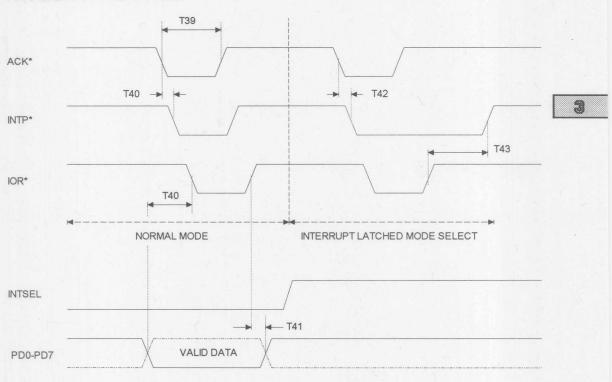


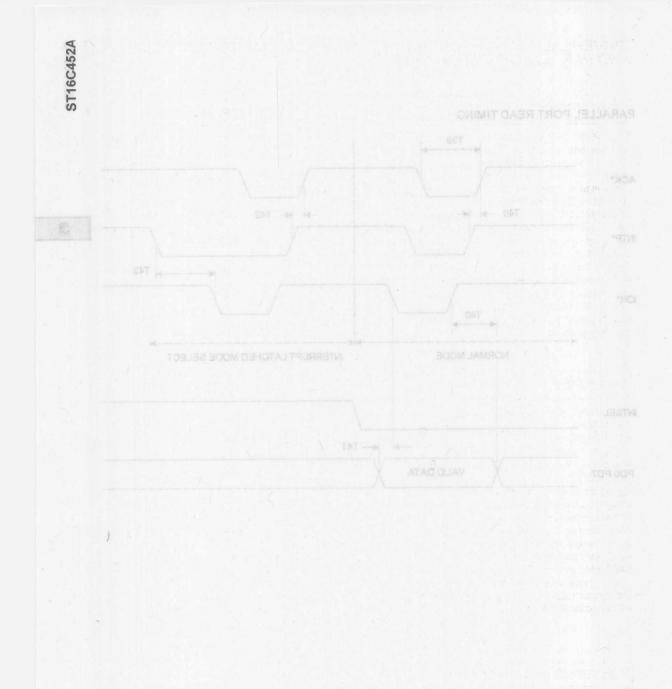




ST16C452AT/PS

PARALLEL PORT READ TIMING





UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFO AND PARALLEL PRINTER PORT

DESCRIPTION

The ST16C552 is a dual universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO and a bi-directional CENTRONICS type parallel printer port. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C552 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C552 provides internal loopback capability for on board diagnostic testing.

The ST16C552 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

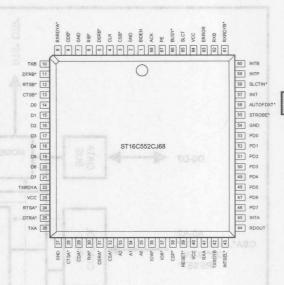
FEATURES

- Pin to pin and functional compatible to VL16C552, WD16C552
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modern control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C550
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source.
- · Bi-directional hardware/software parallel port
- Bi-directional I/O ports

ORDERING INFORMATION

Part number	Package	Operating	temperature
ST16C552CJ68	PLCC	0° C	to + 70° C
ST16C552LI68	PLCC	-40° C	to + 85° C

PLCC Package



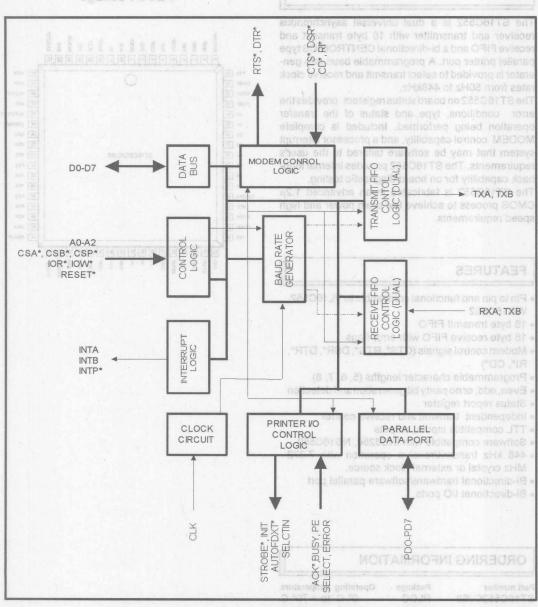
Printed September 8, 199-

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFO AND PARALLEL PRINTER PORT

BLOCK DIAGRAM

PLCC Package

DESCRIPTION



SYMBOL DESCRIPTION

Symbol	Pîn	Signal Type	Pin Description
n. ransmitted via	If no 14-21 (we see the man and the man an	has been detec	significant bit of the data bus and the first serial data bit to be received or transmitted.
The second state of the second	35-33		Address select lines. To select internal registers.
is pin can be	4 (active low). To	I inal ready A/B is ready to c	Clock input. An external clock can be used to clock internal
BIDEN ugluo* g a "0" to that does not have	Owill set the DTR state after writing Note that this pin or receive opera-	i" at the MCR bit ill be set to high after the reset.	Printer direction select. A high puts the parallel port in the input / output mode and low sets the ST16C552 to output mode.
*WOI	36 oni oT (wol evi	l o send A/B (ac	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR* of nig eld tent elon, right	to send. Writing to the set to the set to the set to the set to the transfect on the transf	ntrof redister (M r the reset this p	Read strobe (active low). A low level on this pin transfers the contents of the ST16C552 data bus to the CPU.
RDOUT beviscer (alab	44 erial information 52 receive input	O (Input A/B. The s	Read select out (active high). This pin goes high when the CPU is reading data from the ST16C552 to en/disable the external transceiver or logic's.
RESET* Cons	ice (to 95 s logic r c input is disabled to the TX output	gla one and a spi sack mode the R	
ditions can be	lows, street CTS has considered whose considered cTS has a	notional function	Chip select A/B (active low). A low at this pin enables the serial port-A/B / CPU data transfer operation.
DSR A/B* zsog niq sidT (on. 3,15 state active high interrupt enable	receive operate stout A/B (three renabled by the	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
RI A/B*betoels	iver data availat ondit 6,08 g is on hugh). This pin in 190552 is full, it	moden Islatus c eady A/B (activi	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.

3

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
DO is the feast			Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
TX A/B		d or ir O milted sled lines. To sa	Serial data output A/B. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
reffel port in the	ober 25,11 ober	t baud O te gent egildn select. A t trut mode and in	Data terminal ready A/B (active low). To indicate that ST16C552 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
RTS A/B* beat areland hig a USO ad	the level woll and and area see see	ds of the \$118C5 of out (active high	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
RX A/B	41,62 at	ading data from anyony or log- encostyler or log- et. (ective low) will obtain a register rer input will be d	Serial data input A/B. The serial information (data) received from serial port to ST16C552 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
es pinindicates		t A/3 (bolive lot -A/6 / CPU detait sady A/8 (active) Misready to exc	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
INT A/B vieces	45,60 x 8 1	By a Quilled of	Interrupt output A/B (three state active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
TXRDY A/B	22,42	he modem has i	Transmit ready A/B (active high). This pin goes high when the transmit FIFO of the ST16C552 is full. It can be used as

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
		impose linguit or l	a single or multi-transfer.
RXRDY A/B*	16,6 ne printer ackin w by the printer	output from the p O urpose input or I input is pulsed to	Receive ready A/B (active low). This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.
	38 ive low). To sle	een accepted st I arrupt output (ac pod. This pin to	Parallel printer port chip select (active low). A low at this pin enables the parallel port / CPU data transfer operation.
PD7-PD0 // //g	46-53 dw	MATEON ON SIZE	Bi-directional parallel ports (three state). To transfer data in or out of the ST16C552 parallel port. PD7-PD0 are latched
STROBE*	emi er55*a lliw	o this ON to VOX	General purpose I/O or data strobe output (open drain active low). This output indicates to the printer that valid
AUTOFDXT*	56*	i powe ON ound.	active low). When this signal is low the printer should automatically line feed after each line is printed.
INIT	57*	1/0	General purpose I/O or initialize line printer (open drain active low). When this signal is low, it causes the printer to be initialized.
SLCTIN*	58*	1/0	General purpose I/O or line printer select (open drain active low). When this signal is low, it selects the printer.
ERROR*	63*	WRITE MO	General purpose input or line printer error (active low). This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	65* olds	interrupt En FIFO Contro Line Contro	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	*66 Register	Scratchpad LSS of Divi MSB of Div	General purpose input or line printer busy (active high). An output from the printer to indicate printer is not ready to accept data.

Symbol	PE 67* Instanti-tium o		Pin Description				
PE			General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.				
ACK* no elignic	68*	adyA/6 (active) PO is (Mi. It car					
INTP* Isrago all	7 (elsia sant)	merpon chip se e pare O pon / call pare se sal pare la cons	Printer interrupt output (active low). To signal the state of the printer port. This pin tracks the ACK* input pin, Wher ACK* is low INTP is low and when ACK* is high INTP is high				
unt (open drain	43 tuo edoniz ete pertro reeteori	put mode. uppose I/O or ii). This output incelled at the property	Interrupt select mode. The external ACK can be selected as an interrupt source by connecting this pin to the GND Connecting this pin to VCC will set the interrupt to latched mode, reading the status register of the printer section				
printer should	27). When this sig					
VCC	23,40,64	she bast and ylu	Power supply input.				

^{*} Have internal pull-up resistor on inputs

PROGRAMMING TABLE FOR SERIAL PORTS

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Registe
0	0	1	Camillan huma assame lawness	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	printer has been selected.	Line Control Register
1	0	0	monorabe inpose can learning	Modem Control Register
11	0	1	Line Status Register	1 *88
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0	· · · · · · · · · · · · · · · · · · ·	LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C552 ACCESSIBLE REGISTERS

A2A	1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0	0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0) 1	IER of dome vito	o oga liiw i	SR BITA-	O L (S)	noty flag	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1	1 0	FCR tod neriw e	RCVR trigger (MSB)	RCVR trigger (LSB)	Ompt D) LI	intornal scaledty it is valid the stad	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1		ISR mady medical	0/ FIFOs enabled	0/ FIFOs enabled	E) L4 in the	mo o av galog wo llwcawil	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1	PFIF	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 (0 0	MCR	0	0	0	loop back	INT enable	Not used	RTS*	DTR*
tuobu	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
Magar Magar	1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1	1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0	0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0	0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

DLL and DLM are accessible only when LCR bit-7 is set to "1".

3

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

- A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.
- B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.
- C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C552 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

- A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.
- B) LSR BIT4-1 will specify which error(s) has occurred.
- C) LSR BIT-5 will indicate when the transmit FIFO is empty.
- D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.
- E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C552 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C552 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2¹⁶ -1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modern status registers to the INT output pin.

IER BIT-0; show 022081TS m at \$22081TS north

0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

no more characters in the PIFO. ::TIB RBI

0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:

0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:

0=disable the modem status register interrupt. 1=enable the modem status register interrupt.

IER BIT 7-4:

All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C552 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C552 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

Р	D3	D2	D1	D0	Source of the interrupt
1	0	1	10	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

*RECEIVE TIME-OUT: The first state of the st

This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be: $T = 4 \times 7$ (programmed word length) +12 = 40 bits Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be: $T = 4 \times 7$ (programmed word length) + 12 = 40 bits Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

ISR BIT-0:

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

1=no interrupt pending.

ISR BIT 1-3: Old behald at relogishing that end refle

Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7: Soom OchoorTe mi si SecoenTe medta

These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to "1" in ST16C552 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0: MONEY OF THE STORY OF SHE IN WOLLD HIM

0=Disable the transmit and receive FIFO.

1=Enable the transmit and receive FIFO.

This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:

0=No change, amiT) T at eulay hio

1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2; diliw two emit. Jid gots end bns ytmag en

0=No change.

1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3: Ct + (rffp)(e) brow beminergorg) T X A = T

0=No change. The proposed LOT VON = emily not

1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":

When ST16C552 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":

When ST16C552 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":

When ST16C552 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":

When ST16C552 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5: purjoint yigms retifined and eldene=1

Not used.

FCR BIT 6-7: metmi suista enil revienno entre idealb=0

These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	bits are 40 to logic zero
1	0	08
1	(94) 9	IPT STAPLUS REGISTE

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:

These two bits specify the word length to be transmitted or received.

	jth	d leng	BIT-0	BIT-1
		50	0	001
		6	1	0
16		70	VIO OSA)	6/10
		8	1	1

LCR BIT-2: Show) 93M

The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)		
215010	5,6,7,8 ind	re FIFO, This		
1	5	1-1/2		
1	6,7,8	2		

LCR BIT-3:

Parity or no parity can be selected via this bit, a self. 0=no parity and a land and a material and and

1=a parity bit is generated during the transmission, receiver also checks for received parity.

are set to "0" whenever the CPU reads "1:4-TIA DJ

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.

0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format

1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.

LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:

Break control bit. It causes a break condition to be transmitted (the TX is forced to low state). **/>
Description

O=normal operating condition.

1=forces the transmitter output (TX) to go low to alert the communication terminal.

loop-back mode. It is the compliment o:7-TIB RDL

The internal baud rate counter latch enable (DLEN)... 0=normal operation.

1=select divisor latch register.

MODEM CONTROL REGISTER (MCR) :0-TIS 921

This register controls the interface with the MODEM or a peripheral device (RS232). The relation published

MCR BIT-0:

0=force DTR* output to high mon) rous numero on=0 1=force DTR* output to low: stables, rous numeros

MCR BIT-1: ent reits vino ruoco lliw rone numevo na

0=force RTS* output to high. delegated been entitled at 1=force RTS* output to low. and delegated life and many

MCR BIT-2:

Not used.

MCR BIT-3:

0=set INT output pin to three state mode.
1=set INT output pin to normal / active operating mode.

register is overwritten, but it is not transferred to the

MCR BIT-4:

0=normal operating mode.amon) none primari on=0

1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and INT enable are connected to modem control inputs.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:

Not used. Are set to zero permanently. 38-TIE 9821

LINE STATUS REGISTER (LSR) blod astimenent = 1

This register provides the status of data transfer to CPU.

3

LSR BIT-0: (ROM) RETEIDER LORTINGO MEGOM

0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:

0=no overrun error (normal).

1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:

0=no parity error (normal).

1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:

0=no framing error (normal).

1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:9 (ATC) bas tugni reviscer ent of beiden

0=no break condition (normal).

1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5: the O melbeld a fifte all drug rewelled word

0=transmit holding register is full. ST16C552 will not accept any data for transmission.

1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6: .yimensmeq orax of fee enA .besu told

0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In
FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:

0=Normal. (and noted in approximately setting

1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:

Indicates that the CTS* input to the ST16C552 has changed state since the last time it was read.

MSR BIT-1: Month of between all fid virtual MEVE at

Indicates that the DSR* input to the ST16C552 has changed state since the last time it was read.

MSR BIT-2:

Indicates that the RI* input to the ST16C552 has changed from a low to a high state.

MSR BIT-3: sist beyiever beet bettle and a fire

Indicates that the CD* input to the ST16C552 has changed state since the last time it was read.

MSR BIT-4:

This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:

This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:

This bit is equivalent to MCR bit-2 during local loopback mode. It is the compliment of the RI* input.

MSR BIT-7:

This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C552 provides a temporary data register to store 8 bits of information for variable use.

ST16C552 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0,
	LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0,
	MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR		
50 000	A CANADA A CONTRACTOR OF THE C	TATUS REGIST		
110		0.026		
150	768			
300	384	:0-1 718 91		
600	192			
1200	96			
2400	48	:S-T18 R		
4800	24	nterrupt condition		
7200		= an interrupt is		
9600		his bit will be set		
19.2K	6	toor		
38.4K	3 minned	e no interrupt is		
56K	HATEL 2 IN SUT			
115.2K	1			

SIGNALS		0= ERROR* ing 1= ERROR* ing
TX RTS* DTR* INT RXRDY*		SR BIT-4: SLCT input sta 0= SLCT input 1= SLCT input
TXRDY	Low	SR SIT-5:

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW*	IOR*	
0	0	PORT REGISTER TIS MOS	PORT REGISTER	
0	1	I/O SELECT REGISTER	STATUS REGISTER *	
1	1 8 0 18	CONTROL REGISTER	COMMAND REGISTER	

^{*} Reading the status register will reset the INTP output.

PRINTER PORT REGISTER DESCRIPTIONS

PR BIT 7-0:

PD7-PD0 bi-directional I/O ports.

STATUS REGISTER

This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:

Not used. Are set to "1" permanently.

SR BIT-2:

Interrupt condition.

0= an interrupt is pending

This bit will be set to "0" at the falling edge of the ACK* input.

1= no interrupt is pending

Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:

ERROR* input state.

0= ERROR* input is in low state

1= ERROR* input is in high state

SR BIT-4:

SLCT input state.

0= SLCT input is in low state

1= SLCT input is in high state

SR BIT-5:

PE input state.

0= PE input is in low state

1= PE input is in high state

SR BIT-6:

ACK* input state.

0= ACK* input is in low state

1= ACK* input is in high state

SR BIT-7:

BUSY input state.

0= BUSY input is in high state

1= BUSY input is in low state

COMMAND REGISTER

The state of the STROBE*, AUTOFDXT*, INIT, SLCTIN* pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0: betarenen al trumelal auteta-MEGOM

STROBE* input pin.

0= STROBE* pin is in high state

1= STROBE* pin is in low state

COM BIT-1:

AUTOFDXT* input pin.

0= AUTOFDXT* pin is in high state

1= AUTOFDXT* pin is in low state

COM BIT-2:

INIT input pin.

0= INIT pin is in low state

1= INIT pin is in high state

COM BIT-3:

SLCTIN* input pin.

0= SLCTIN* pin is in high state

1= SLCTIN* pin is in low state

COM BIT-4:

Interrupt mask.

0= Interrupt (INTP output) is disabled

1= Interrupt (INTP output) is enabled

COM BIT 7-5:

Not used. Are set to "1" permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE*, AUTOFDXT*, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:

STROBE* output control bit.

0= STROBE* output is set to high state

1= STROBE* output is set to low state

CON BIT-1:

AUTOFDXT* output control bit.
0= AUTOFDXT* output is set to high state
1= AUTOFDXT* output is set to low state

CON BIT-2:

INIT output control bit.

0= INIT output is set to low state

1= INIT output is set to high state

CON BIT-3:

SLCTIN* output control bit.
0= SLCTIN* output is set to high state
1= SLCTIN* output is set to low state

CON BIT-4:

Interrupt output control bit.

0= INTP output is disabled

1= INTP output is enabled

CON BIT-5:

I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit. 0= PD7-PD0 are set for output mode 1= PD7-PD0 are set for input mode **CON BIT 7-6:**

Not used.

I/O SELECT REGISTER

Software controlled I/O select.

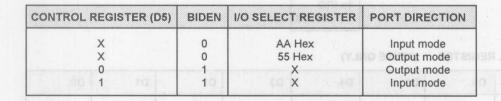
Bi-directional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one"

Hardware/software I/O select.

Bi-directional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or "55" Hex for output.

ST16C552 EXTERNAL RESET CONDITION

SIGNALS	RESET STATE
PD0-PD7 STROBE* AUTOFDXT* INIT SLCTIN*	Low, output mode High, output mode High, output mode Low, output mode High, output mode



ST16C552 PRINTER PORT REGISTER CONFIGURATIONS

PORT RE	EGISTER	(READ/WF	RITE)				
D7	D6	D5	D4	D3	D2	D1	D0
PD7niger	PD6	PD5	PD4	PD3	PD2	PD1 _{id} lost	
		(READ ON					INIT output is N BIT-3: CTIN* output
D7	D6	D5	D4	D3	D2	D1	D0
BUSY*	ACK TES	зя РЕляэтх	SLCT	ERROR STATE	IRQ	1 did-lotted	1-TIE W
СОММА		R (READ ON	PD0-PD7 USTROBE* AUTOFDXI	belooled	0= Interru	tion of the PDT	a-TIB II
D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN*	INIT	AUTO- FDXT*	STROBE
	ион	PORT BIREC	0= IRQ disabled 1= IRQ enabled	no sereci	изоне		
CONTRO		lom (WRITE O		AA /			
D7	D6	D5	D4	D3	D2	D1	D0
	-	I/O SELECT	IRQ MASK	SLCTIN*	INIT	AUTO- FDXT*	STROBE
	0=Output 1=Input		0=INTP out disabled 1=INTP out enabled				

AC ELECTRICAL CHARACTERISTICS

 $\rm T_{A} = 0^{\circ}$ - 70° C, Vcc=5.0 V \pm 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
						ckaga dissipation
T,	Clock high pulse duration	50	aom	TERM	ns	V Januarna (a s
T.	Clock low pulse duration	50	CONTRACTOR OF STREET	PRATE A S	ns	External clock
T.	Clock rise/fall time			10	ns	
T.	Chip select setup time	5	ne manage	esamu	ns	0°-70° C, Vcc=5.0
T ₂ T ₃ T ₈ T ₉	Chip select hold time	0			ns	
T ₁₂	Data cotun tima	15			ns	
T ₁₃	Data hold time	15		1625	ns	1odrny
T ₁₄	IOW* delay from chip select	10			ns	
T ₁₅	IOW* strobe width	50		Total Maria	ns	
T 15	Chip select hold time from IOW*	0			ns	V _{LCK} Clock inpu
T ₁₆	Write cycle delay	55		Vis	ns	Visce Clack input
T ₁₇	Data hold time	15			1075	V I Input low I
T ₁₉	IOR* delay from chip select	10			ns	V _H input high
T ₂₁	IOR* strobe width	65			ns	Vo. Output low
T ₂₃		0			ns	
T ₂₄	Chip select hold time from IOR*	55			ns	
T ₂₅	Read cycle delay				ns	
Tr	Read cycle=T ₂₃ +T ₂₅	115	Page 11	0.5	ns	400 - 51
T ₂₆	Delay from IOR* to data			35	ns	100 pF load
28	Delay from IOW* to output			50	ns	100 pF load
T ₂₉	Delay to set interrupt from MODEM input			70	ns	100 pF load
T ₃₀	Delay to reset interrupt from IOR*			70	ns	100 pF load
T ₃₁	Delay from stop to set interrupt			1 _{Rclk}	ns	100 pF load
T ₃₂	Delay from IOR* to reset interrupt			200	ns	100 pF load
T ₃₃ Am	Delay from initial INT reset to transmit start	8		24	*	
T ₃₄	Delay from stop to interrupt			100	ns	
T ₃₅	Delay from IOW* to reset interrupt			175	ns	
T ₃₉	ACK* pulse width	75			ns	
T ₄₀	PD7 - PD0 setup time	10			ns	
14	PD7 - PD0 hold time	25			ns	
T ₄₂	Delay from ACK* low to interrupt low	5			ns	
T ₄₃	Delay from IOR* to reset interrupt	5			ns	
T ₄₄	Delay from stop to set RxRdy			1 _{RCLK}		
T ₄₅	Delay from IOR* to reset RxRdy			'RCLK	μS	
T ₄₆	Delay from IOW* to set TxRdy		Mark Mark	195	ns	loo I Avg powe
T ₄₇	Delay from start to reset TxRdy			8	*	I, Input leaks
47	Boldy Holli Start to leset Txixdy			U	age	for Clock leaf
N	Baud rate devisor	1		216-1	Hop resis	R _{IX} — Internal pti



Note 1 * = Baudout* cycle

ABSOLUTE MAXIMUM RATINGS

AC ELECTRICAL CHARACTERISTICS

Clock high pulse duration

Note 1 *= Baudout* cycle

Supply range		rwise specified.	OND ON A THIRE S OTHER		7 Vo	
Voltage at any pin	-		GND-0.3 V	to	VCC+0.3	V
Operating temperature	etio()	(imite	nalemense), C	to +70°	C
Storage temperature		Min Typ Max	-40	° C	to +150°	C
Package dissipation					500 m	W

DC ELECTRICAL CHARACTERISTICS

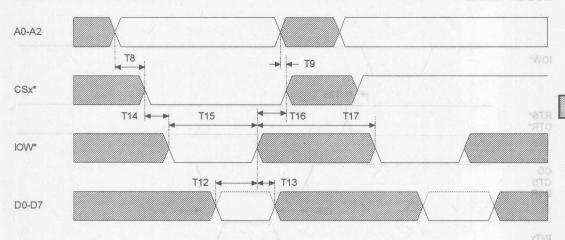
 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol		Paran	neter	Min	Limits Typ	Max	Units	Conditions
VILCK VIHCK VIL VIH VOL	Clock input Clock input Input low le Input high I Output low	low leve high leve evel evel		-0.5 3.0 -0.5 2.2	*WC	0.6 VCC 0.8 VCC 0.4	mi V im	T Chip select Chip select Chip select T Chip
b b	seel 3q 00 r seel 3q 00 r seel 3q 60 r seel 3q 00 r Output high	an a	35 50 50 70 100 200 100	2.4 3 3 0 6 8 7	IOR* IOR* broupt o transm terrupt rrupt low	fata output from N output from N oset interr freset interrupt reset in v oset interrupt	stop to it IOW* to width setup time hold time IOK* to	I_{OL} = 20.0 mA PD7-PD0 I_{OL} = 10 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OL} = 6.0 mA on all other outputs I_{OH} = -6.0 mA D7-D0 I_{OH} = -12.0 mA PD7-PD0 I_{OH} = -0.2 mA SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{OH} = -6.0 mA on all other outputs
I _{CC} I _{IL} I _{CL} RIN	Avg power Input leaka Clock leaka Internal pul	ge age	8 681	4	12 yb		IIIA	Tage of the control o

3

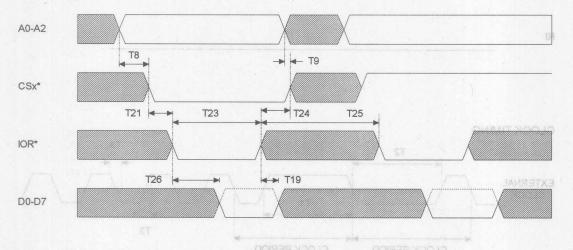


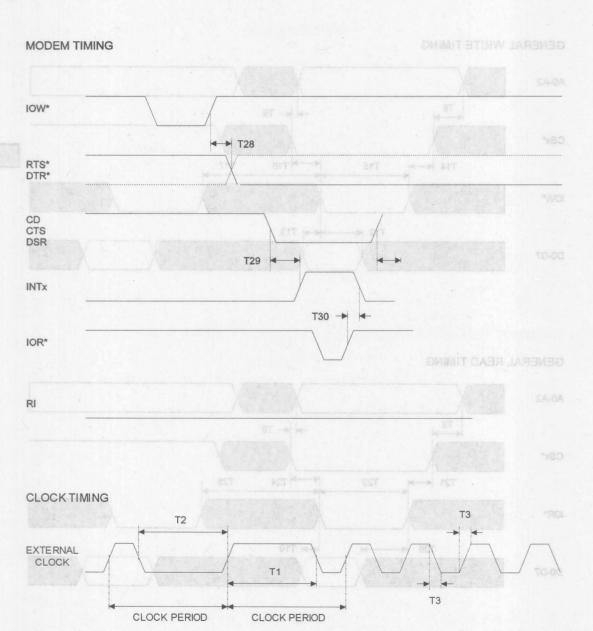
MODEM TIMING

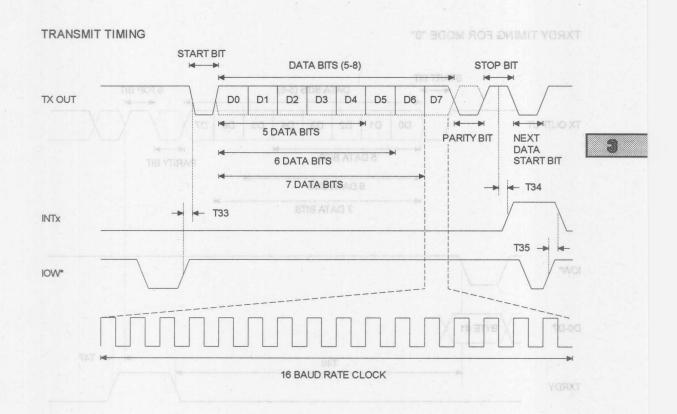


→ <- 08T

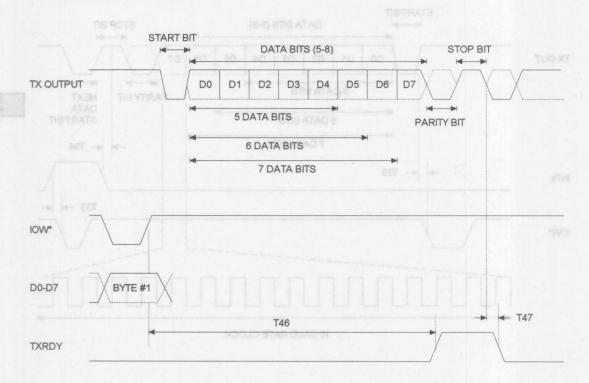
GENERAL READ TIMING

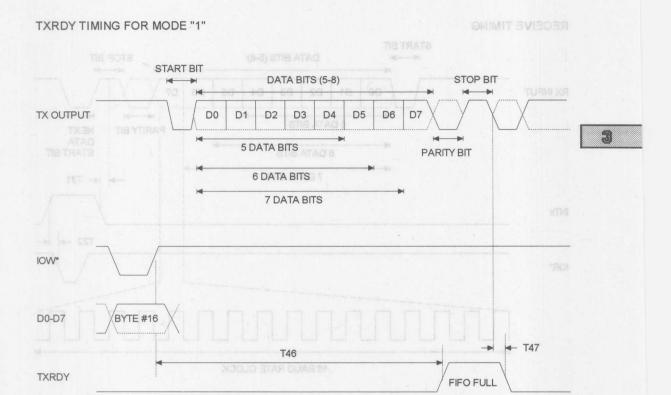


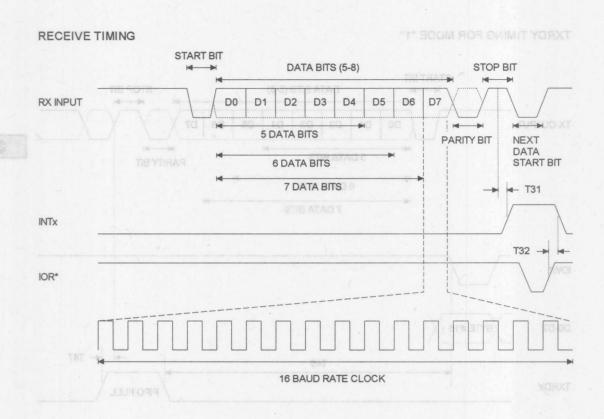




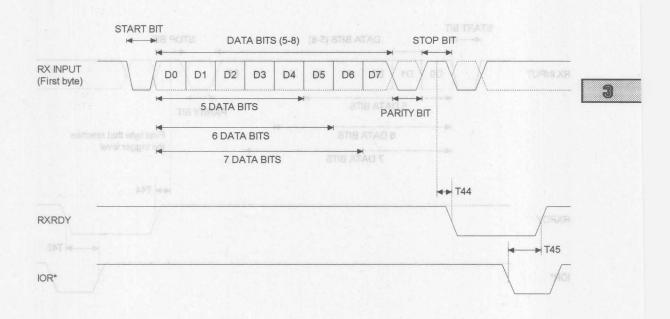
TXRDY TIMING FOR MODE "0"





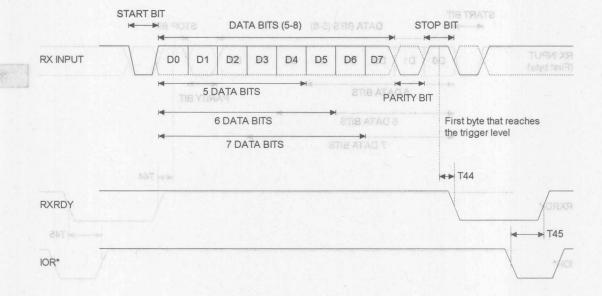


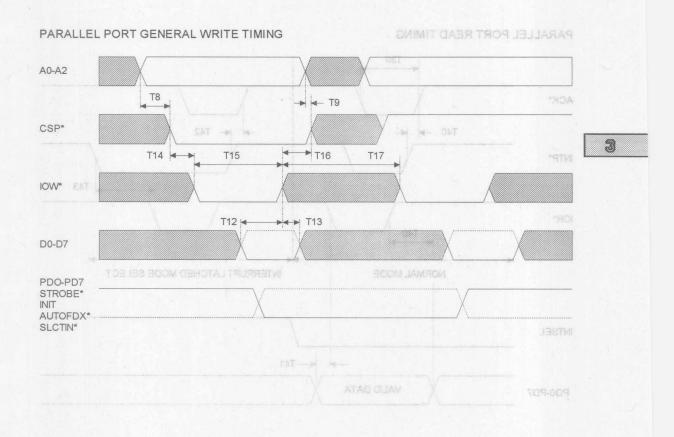
RXRDY TIMING FOR MODE "0"

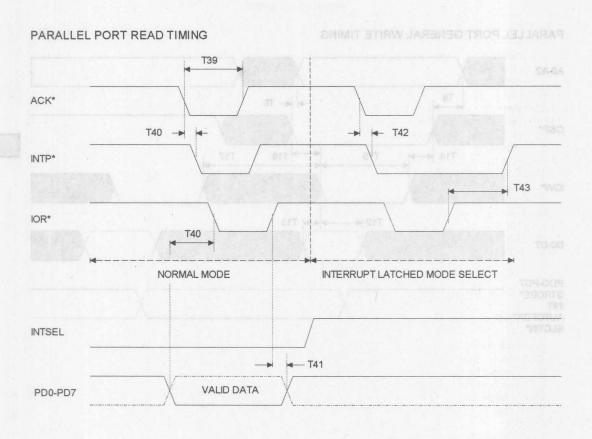


RXRDY TIMING FOR MODE "1"

RXRDYTIMING FOR MODE "8"









ST16C553

Printed September 8, 1994

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFO AND PARALLEL PRINTER PORT WITH 83 BYTE FIFO

DESCRIPTION

The ST16C553 is a dual universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO and a bi-directional CENTRONICS type parallel printer port with 83 bytes of FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz.

The ST16C553 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C553 provides internal loopback capability for on board diagnostic testing.

The ST16C553 is fabricated in an advanced 1.2μ CMOS process to achieve low drain power and high speed requirements.

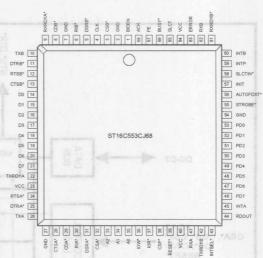
FEATURES

- Pin to pin and functional compatible to VL16C552, WD16C552
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- 83 bytes of printer output FIFO
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- · Status report register
- Independent transmit and receive control
- TTL compatible inputs, outputs
- Software compatible with INS8250, NS16C550
- 448 kHz transmit/receive operation with 7.372 MHz crystal or external clock source.
- · Bi-directional hardware/software parallel port
- · Bi-directional I/O ports

ORDERING INFORMATION

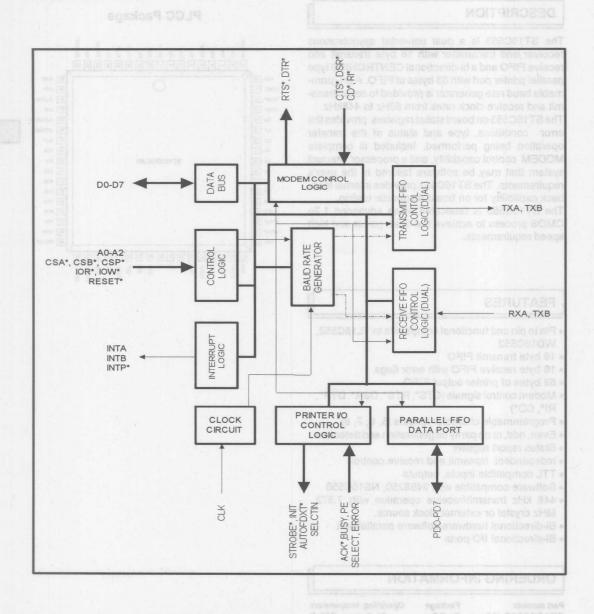
Part number ST16C553CJ68 ST16C553IJ68

Package PLCC PLCC Operating temperature 0° C to + 70° C -40° C to + 85° C PLCC Package



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BLOCK DIAGRAM



Symbol	Pin	Signal Type	Pin Description
n, ransmitted via		NO A too so to	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. Do is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
A0-A2		mark (high) stans	Address select lines. To select internal registers.
CLK tant etapibni d ed neo nig ati	4 T (we low). T eive date. T	when the transmit I linet ready AVB (s i is ready to red	Clock input. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
BIDEN COM OF STATE OF		t" autholistic bit of it be set to high a ofter the reset. V	Printer direction select. A high puts the parallel port in the input / output mode and low sets the ST16C553 to output mode.
*WOI	36	on the transmit or I o send A/B (active	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR* and end	tes lim 37 and 9 of tes ed lim r	otrot redister (MC) L'Ore reset this pin	Read strobe (active low). A low level on this pin transfers the contents of the ST16C553 data bus to the CPU.
RDOUT	44 notismont isi	es not have any lat	Read select out (active high). This pin goes high when the CPU is reading data from the ST16C553 to en/disable the external transceiver or logic's.
RESET*	olgo (39 el) e aldsalb ar lugni	port to ST13Ct55 gicone Ind a spro nack mode the RI and connected to	Master reset (active low). A low on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
		evitos) el A bres control function in	Chip select A/B (active low). A low at this pin enables the serial port-A/B / CPU data transfer operation.
DSR A/B*	31,5 Inin evitos erei eluane igimen	ading the MSR 31 receive operation upput A/B (three seabled by the in	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
RI A/B*	ang 30,6 mg	eiver error, receiv modem [†] status ca eady A/B (active i It FFO of the ST1	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.

3

Symbol	Pin	Signal Type	Pin Description
DO is the least	da e 29,8 d l/k UPO ant mod		Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modern.
TX A/B	26,10	d or b osmitted	Serial data output A/B. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
allel port in the	inic 25,11 de se la companya de la c	baud o le gen action select. A l put mode and fo	Data terminal ready A/B (active low). To indicate that ST16C553 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
A'B* 1998 a pin transfers the CPU	the level on the total on the t	f the COJ data I be (active low) its of the ST16C	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
RX A/B ent its feasiling bits fuction ref	41,62	ensceiver or log let (aglive low). X d internal registe	
in. is pin indicates	w. A low on the sale with a constant work. A low on the sale with	A/B / OPU data	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
niq sint no wel	A (wol evisos)	ave ano affect of the state of	Interrupt output A/B (three state active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
TXRDY A/B	22,42	0 911	Transmit ready A/B (active high). This pin goes high when the transmit FIFO of the ST16C553 is full. It can be used as

Symbol	Pin	Signal Type	Pin Description
		urpose input or	a single or multi-transfer.
RXRDY A/B*	9,61 ne printer ackin w by the printer	output from the last or long input is putsed to	Receive ready A/B (active low). This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.
	38 pia oT. (wal svi	neen accepted si I emupt output (ad r pod. This pin to	Parallel printer port chip select (active low). A low at this pin enables the parallel port / CPU data transfer operation.
PD7-PD0	1 e 46-53	ons wo I/O T/A w	or out of the ST16C553 parallel port. PD7-PD0 are latched during output mode.
STROBE*	55* H	rupt source by a grain ON to VCC adding the status INTP output.	General purpose I/O or data strobe output (open drain
AUTOFDXT*	56*	bound I/O wood to	General purpose I/O or automatic line feed (open drain active low). When this pin this signal is low, the printer should automatically line feed after each line is printed.
INIT	57*	I/O	General purpose I/O or line printer initialize (open drain active high). To signal the line printer to enter internal initialization routine.
SLCTIN*	58*	1/0	General purpose I/O or line printer select (open drain active low). When this signal is low, it selects the printer.
ERROR*	63*	WESTERNO Transmit Ha	General purpose input or line printer error (active low). This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	65*	Interrupi En FIFO Contro Line Contro Modern Con	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	66*	I Scratchpad LSB of Divi	General purpose input or line printer busy (active high). An output from the printer to indicate printer is not ready to accept data.

3

Symbol	Pin	Signal Type	Pin Description
PE	67*	r multi-t†ansfer.	General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.
		eady A/B (active)	RXRDY A/B* 9,61 O Receive r
ACK* 10 signiz	8 28 68*J 9d	FO is full, it can	General purpose input or line printer acknowledge (active low). This input is pulsed low by the printer to indicate that data has been accepted successfully.
A low at this pin		inter port chip sere	CSP* Parallel pr
d transfer deta in		ie para O I port / C nal parallel ports (se ST16C553 par	the printer port. This pin tracks the ACK* input pin, When ACK* is low INTP is low and when ACK* is high INTP is high
INTSEL*	43	put mode.	
orinter that valid		urpose I/O or b). This output ind allable at the primal	Connecting this pin to VCC will set the interrupt to latched
low, the printer	this signal is	r). When this pin	Signal and power ground. **TXGHOTUA **DXGHOTUA **POWER Supply input.

^{*} Have internal pull-up resistor on inputs of digital syllas

PROGRAMMING TABLE FOR SERIAL PORTS

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1.	a politica bissoci escapion ferenza Co	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	printer has been selected.	Line Control Register
1	0	0	printer has been selected.	Modem Control Register
1.	0	1	Line Status Register	+00
1	nier is i	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0	acoopt uarm.	LSB of Divisor Latch
0	0	1		MSB of Divisor Latch

ST16C553 ACCESSIBLE REGISTERS A/B

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
1 0 0 error(s) ha	Is DIER IS I	FIFO.	LSR BIT red.	0 A) in t 8 c Cur	rangonille ng registe nsmitter i nsmit shi uld be per	modem status interrupt	receive line status	transmit holding register interrupt	receive holding registe
0 1 0	FCR and name ats	RCVR trigger (MSB)	RCVR trigger (LSB)	(0 0 me l	em oy lia ver lotema 16 x slook	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR ISR IS	0/ FIFOs enabled	0/ FIFOs enabled	(G o b	bit o vali of the star peiver from a low goin	int priority bit-2	int priority bit-1	int priority bit-0	int status
1 1 0 step FIFO e	LCR owl everl of viscen side	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
0 0 1	MCR STAR GU	O (ABLE BA	0 OGRAMN	. 0 99 . s	loop back	INT enable	not used	RTS*	DTR*
1 0 1 nable Baud i any clock ny divisor i	R2J s a program ble of takin iding it by	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
111	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

DLL and DLM are accessible only when LCR bit-7 is set to "1".

3

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

- A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.
- B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.
- C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C553 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

- A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.
- B) LSR BIT4-1 will specify which error(s) has occurred.
- C) LSR BIT-5 will indicate when the transmit FIFO is empty.
- D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.
- E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

The ST16C553 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C553 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-8 MHz and dividing it by any divisor from 1 to 2¹⁶-1. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:

0=disable the receiver ready interrupt.

IER BIT-1: riw (evitosni) do fligh (inactive) which believe at it

0=disable the transmitter empty interrupt. 9 000 011 1=enable the transmitter empty interrupt.

IER BIT-2:

0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:

0=disable the modem status register interrupt. 1=enable the modem status register interrupt.

IER BIT 7-4: 1900 to O FIF

All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C553 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C553 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

Р	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Sta-
			dip	nel b	tus Register)
2	0	1	0	0	RXRDY (Received Data
		10.0		8	Ready)
2*	1	1	0	0	RXRDY (Receive Data
	13	1300		7	time out)
3	0	0	1	0	TXRDY(Transmitter
	1	-			Holding Register Empty)
4	0	0	0	0	MSR (Modem Status
					Register)

*RECEIVE TIME-OUT: Does impossible

This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:

T = 4 X 7(programmed word length) +12 = 40 bits

Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:

T = 4 X 7(programmed word length) + 12 = 40 bits

Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters

ISR BIT-0:

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

1=no interrupt pending. 9ff helaigh guiblor firmment (subset) from the line YURXT off evuse continued to the continued to the

ISR BIT 1-3: old bebed a reformed test ent refte

Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7: sbom 02408172 ni si 22206172 nertW

These bits are not used and are set to zero in ST16C450 mode. BIT 6-7: are set to "1" in ST16C553 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0: reflect OFIF short to and if wol ad Illw

0=Disable the transmit and receive FIFO.

1=Enable the transmit and receive FIFO.

This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1: problem evisors smit does to bevisoes

0=No change. The sales to emit lautes of

1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2: He two emit tid gold end one vineg on

0=No change.

1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3: + (nipped brow bemmargorg) T X h = T

0=No change.

1=Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":

When ST16C553 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":

When ST16C553 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":

When ST16C553 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":

When ST16C553 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:

Not used.

FCR BIT 6-7: etni cuteta enil reviscer esti eldene=1

These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-6	FIFO trigger level
0	01
1	04
(REO MEN	UPTS 80 US REGIS
1	14
	0

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Wor	rd le	ngth	
0	0	Ready	5		
0	risod(R)	RXRON	6		
1	0	time or	7		
rei1ma	ner1	TXRD	8		

LCR BIT-2: svenerity and of hea at life shift about ORIG

The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)		
31 FO_1 to	5,6,7,8	ne FIO. This		
1	5	1-1/2		
1	6,7,8	2		

LCR BIT-3:

Parity or no parity can be selected via this bit.

0=no parity

1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4: I sheer UPO ent revenents "0" or jes one

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.

0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.

1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.

LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:

Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).

0=normal operating condition.

1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:0 Inemigmoo edi zi il .ebom boad-gool

The internal baud rate counter latch enable (DLEN). 0=normal operation.

1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:

0=force DTR* output to high.
1=force DTR* output to low.

MCR BIT-1:

0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2: 30 717 tino beligme saw reisiger gniblori

Not used. If any name wino puodo lliw none numevo ne

MCR BIT-3: elements lent stold retainer filds ent ni

0=set INT output pin to three state mode.

1=set INT output pin to normal / active operating mode.

MCR BIT-4:

0=normal operating mode.

1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR bit-2 and INT enable are connected to modem control inputs

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:

Not used. Are set to zero permanently.

3

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:

0=no data in receive holding register or FIFO.

1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:

0=no overrun error (normal).

1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:

0=no parity error (normal).

1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

disabled, internally the transmitter out: E-TIB RSJ

0=no framing error (normal).

1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4: algumetri enti tud Jenoiterego cele ens

0=no break condition (normal).

1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:

0=transmit holding register is full. ST16C553 will not accept any data for transmission.

1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:

0=transmitter holding and shift registers are full. 1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:

O=Normal. (state of the brown of the state)

1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:

Indicates that the CTS* input to the ST16C553 has changed state since the last time it was read.

MSR BIT-1: migrative between all fid wines MEVE = 1

Indicates that the DSR* input to the ST16C553 has changed state since the last time it was read.

MSR BIT-2:

Indicates that the RI* input to the ST16C553 has changed from a low to a high state.

MSR BIT-3: afab bevieces bas bettimzned eath at "h"

Indicates that the CD* input to the ST16C553 has changed state since the last time it was read.

MSR BIT-4:

This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:

This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:

This bit is equivalent to MCR bit-2 during local loop-

back mode. It is the compliment of the RI* input.

MSR BIT-7:

This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C553 provides a temporary data register to store 8 bits of information for variable use.

ST16C553 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0,
	LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0,
	MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0
AFR	AFR BIT 0-7=0

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
	2304	
	1047	
	768	
	384	
600	192 And	nds with either
1200	96	
2400	48	STIBOSSOWIN
4800	24	RI TIMI TO JOSE
7200	16	transfer to in
9600	121	ter without any
19.2K	netmon6envd OF	contains a Fi
38.4K	lamer a3 vd to re	nt of the numb
56K	ehuoo 2 d O IF	2.77
115.2K	i aritho dista to as	at or by a charge
Water to the second of the	The second second second second second	The second second second

SIGNALS	RESET STATE
TX ni woi ni	High I priority da
RTS*	High and high
DTR*	
INT	Three state mode
RXRDY*	High see of shaw
TXRDY	Low Dalliw anshing

PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW*	IOR*
0	0	PORT REGISTER	PORT REGISTER
0	1	I/O SELECT REGISTER	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER
1	1	ALTERNATE FUNCTION REGISTER	FIFO BYTE COUNT REGISTER

^{*} Reading the status register will reset the INTP output. OPIN NOT TO BESTARI YOUR TO SELL ON THE PROPERTY OF THE PROPERTY OF

PRINTER FUNCTIONAL DESCRIPTION

The ST16C553 parallel port is designed to operate as a normal CENTRONICS printer interface. The port contains 83 byte FIFO that may be enabled via bit-7 of the Alternate Function Register (AFR). After reset, the FIFO is disabled and the part will function identical to the ST16C552. Once the FIFO is enabled via AFR bit-7, the port will enter FIFO mode after the first byte of data is strobed to the printer and the printer responds with either an ACK* or BUSY signal.

The ST16C553 will remain in FIFO mode until the part is reset or INIT is brought low. While in FIFO mode, data transfer to the printer will be controlled by the printer without any user intervention. The printer port also contains a FIFO byte counter that maintains a count of the number of bytes remaining in the FIFO. The FIFO and the FIFO byte counter are cleared by a reset or by a change of state of the INIT pin. All FIFO related timing is derived from the clock input to pin 4 of the part.

A special parallel port write / read mode is activated when INIT is held low, either by writing a "0" to Control Register bit-2 or by forcing the INIT pin low. In this mode the FIFO read pointer is advanced by reading the parallel port instead of the ACK* or BUSY signals. The STROBE* output is forced high. This allows the user to perform write to parallel port and read from parallel port operations without strobing data to the printer.

Following an INIT, the parallel port will not be in the FIFO mode. Control Register bit-0 is used as the STROBE*, Status Register bit-7 is the inverse of the BUSY signal, and INTP* is derived from ACK*. The transition into FIFO mode will occur after the first STROBE* is generated and the printer responds with either an ACK* or BUSY. In FIFO mode, STROBE* is generated automatically and writing to Control Register bit-0 has no effect on STROBE*. Alternate Function Register bit 0-2 are used to control the delay and width of STROBE*. Handshaking between the printer and the ST16C553 may be controlled by bit-3 of the Alternate Function Register. Setting this bit to a "1" will result in the use of BUSY instead of ACK* for FIFO

reading and interrupt control. INTP* will transition low when a "1" is written to Control Register bit-0 and will transition high when a write to parallel port is performed. In FIFO mode, data transfer to the printer will be controlled by the printer and will occur at the printer's maximum data rate.

The FIFO byte counter is incremented one count for each parallel port write and decremented one count for each FIFO read (data taken by printer). A FIFO read will be generated at the falling edge of either ACK* or BUSY. The byte counter will require two to three clock cycles to update. Hence, a read to Fifo Byte Count Register (FBCR) should only be performed minimum of three clock after the falling edge of either ACK* or BUSY. The counter is reset whenever the FIFO is reset. If write to parallel port operation is attempted when the FIFO is full, the data will not be written into the FIFO and the counter will not increment.

Two interrupt modes are available and are selected with the INTSEL* pin. If this pin is tied high, a latched interrupt will result. In this mode, INTP* will transition low when a "1" is written to Control Register bit-0. A reset or reading the Status Register will clear the interrupt. If INTSEL* pin is tied low, INTP* will transition low when a "1" is written to Control Register bit-0 and will transition high when a write to the parallel port is issued. This (non-latched) interrupt signal is always available in Status Register bit-6 regardless of the state of the INTSEL* pin. Status Register bit-2 will always contain the latched interrupt state. The polarity of the INTP* pin may be inverted by setting Alternate Function Register bit-6 high.

The ST16C553 provides additional programmable interrupt output options by programming the Alternate Function Register bit 4-5. INTP* output can be selected as FIFO full or FIFO empty interrupt.

PRINTER PORT REGISTER DESCRIPTIONS

PORT REGISTER donut tourism agnada bas *9TML

Bi-directional printer port.

Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports. Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:

PD7-PD0 bi-directional I/O ports.

STATUS REGISTER

This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:

This bit is set to "1" normally except when interrupt is selected as FIFO empty via AFR.

SR BIT-2:

Interrupt condition.

0= an interrupt is pending

This bit will be set to "0" at the falling edge of the ACK*

1= no interrupt is pending looles at hig bugal Y2U8 =1

Reading the STATUS REGISTER will set this bit to

Internot type. State of the tNTP* output p::C-TIB 92

ERROR input state; priwellot ent to ena tot befores

0= ERROR input is in low state

1= ERROR input is in high state

98 98 1141 1110 1110 1111 1118 8-118

SLCT input state.

0= SLCT input is in low state

1= SLCT input is in high state

SR BIT-5:

PE input state.

0= PE input is in low state

1= PE input is in high state

SR BIT-6:

ACK* input state. sidene ai (jugtuo STMI) tournotel =1

0= ACK* input is in low state

1= ACK* input is in high state

SR BIT-7:

BUSY or FIFO full/ FIFO empty signal.

ST16C552 mode (FIFO is not enabled).

0= BUSY input is in high state

1= BUSY input is in low state and sign also in Journal of

FIFO is enabled.

0= FIFO is full

1= One or more empty locations in FIFO 80978 =0

COMMAND REGISTER

The state of the STROBE*, AUTOFDXT*, INIT, SLCTIN* pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:

STROBE* input pin.

0= STROBE* pin is in high state les al Jugluo TIVII =0

1= STROBE* pin is in low state | too al fuotuo TIMI =1

COM BIT-1:

0= AUTOFDXT* pin is in high state

1= AUTOFDXT* pin is in low state uplus 1/110_12 =1

COM BIT-2:

INIT input pin.

0= INIT pin is in low state baldsalb at higher 9TM =0

1= INIT pin is in high state beldans at tugtuo 9TMI =1

COM BIT-3:

NO select, Direction of the PDY-PD.niq tuqni *NITOJS

0= SLCTIN* pin is in high state prince to guilles vd

1= SLCTIN* pin is in low state of lea ene DOR-XOR =0



COM BIT-4:

Interrupt mask.

0= Interrupt (INTP output) is disabled

1= Interrupt (INTP output) is enabled

COM BIT 7-5:

Not used. Are set to "1" permanently.

CONTROL REGISTER. TO ONE A MICH CONTROL REGISTER.

Writing to this register will set the state of the STROBE*, AUTOFDXT*, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:

STROBE* output control bit.

0= STROBE* output is set to high state

1= STROBE* output is set to low state

CON BIT-1:

AUTOFDXT* output control bit.

0= AUTOFDXT* output is set to high state

1= AUTOFDXT* output is set to low state

CON BIT-2:

INIT output control bit.

0= INIT output is set to low state

1= INIT output is set to high state

CON BIT-3:

SLCTIN* output control bit.

0= SLCTIN* output is set to high state XQFOTUA =0

1= SLCTIN* output is set to low state

CON BIT-4:

Interrupt output control bit.

0= INTP output is disabled (three state mode)

1= INTP output is enabled a set a double and Tile 1=1

CON BIT-5:

I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.

0= PD7-PD0 are set for output mode

1= PD7-PD0 are set for input mode

CON BIT 7-6:

Not used.

ALTERNATE FUNCTION REGISTER (AFR)

This register En/Disables FIFO operation and provides additional capabilities to control STROBE*. INTP* and change interrupt functions.

AFR BIT 0-2:

Timing select.

The STROBE* delay and width can be controlled by these bits. I've from from profit of the second mode will be second or the second or t

AFR Bit-2	AFR Bit-1	AFR Bit-0	TSD (clocks)	TSW (clocks)
1	0	0	3	2
1	0	1	5 18	ATLA REC
atu1luo	191110	0	a srif 5 bivor	a reikster a
1	1	1	moiti 9 ico Jq	8 1
0	0	0	6	4
0	0	1	10	8 8
0	thi 1edy	0 /3	10	s bit8s set s
0	1	1FA	1 V 118 0	16

AFR BIT-3:

Interrupt source.

0= ACK* input pin is selected as printer handshaking

1= BUSY input pin is selected as printer handshaking Source and less the RECISTER will set into sor

AFR BIT 4-5:

Interrupt type. State of the INTP* output pin can be selected for one of the following options.

Bit-5	Bit-4	INTP* output	SR bit-0	SR bit-6
0	0	Normal mode	rol1ii	BUSY*
0	1	FIFO empty	111	FIFO empty
1	0	FIFO full	1	FIFO full
1	1	FIFO empty	0	FIFO empty

3

AFR BIT-6:

INTP* output polarity.
0= Normal. INTP* output follows the ACK* input
1= Inverted INTP* output

AFR BIT-7:

FIFO enable / disable function.
0= FIFO is disabled(default mode). The ST16C552 compatible mode.
1= FIFO is enabled. Internal 83 byte of FIFO is enabled.

FIFO BYTE COUNT REGISTER (FBCR)

State and content of the printer FIFO can be monitored by reading this register.

FCBR BIT 0-6:

FIFO byte count. Number of characters left in FIFO.

FBCR BIT-7: FIFO state. 0= FIFO is enabled 1= FIFO is disabled

I/O SELECT REGISTER

Software controlled I/O select.

Bi-directional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one"

Hardware/software I/O select.

Bi-directional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or "55" Hex for output.

ST16C553 EXTERNAL RESET CONDITION

SIGNALS	RESET STATE					
PD0-PD7 STROBE* AUTOFDXT*	Low, output mode High, output mode High, output mode	1 1	×			
INIT SLCTIN*	Low, output mode High, output mode					

PARALLEL PORT DIRECTION SELECT REGISTER (WRITE ONLY)

CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER	PORT DIRECTION
X	0	AA Hex	Input mode
X	0	55 Hex	Output mode
0	1	X	Output mode
1	1	×	Input mode

ST16C553 PRINTER PORT REGISTER CONFIGURATIONS

A2	A	.1	A0	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
X	()	0	PR tools	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
X				STR STR	BUSY*/ Alternate function	ACK	PE	SLCT	ERROR	IRQ	.abd	ipatible mit PIPC is e bied.
X	(0	1	1/0	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
X			0	COM	1 JAMPST	1 X3 caao	1 erte	IRQ state	SLCTIN*	INIT	AUTO- FDXT*	STROBE*
X		1	0	CON	seah	алдал	I/O select	IRQ mask	SLCTIN*	TINI er of cha	AUTO- FDXT	STROBE*
X		1	1	AFR short so		INTP* polarity	IRQ type bit-1	IRQ type bit-0	INTP* source	TIMING select bit-2	TIMING select bit-1	TIMING select bit-0
X		1	1	FBCR	FIFO* status	FBC-6	FBC-5	FBC-4	FBC-3	FBC-2	FBC-1	FBC-0

 CONTROL REGISTER (ps)
 BIDER
 NO SELECT REGISTER
 PORT DIRECTION

 X
 0
 AA Hex
 Input mode

 X
 0
 55 Hex
 Output mode

 0
 1
 X
 Output mode

 1
 X
 Input mode

 1
 X
 Input mode

AC ELECTRICAL CHARACTERISTICS

T₄=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified. Salvianto against a V 0.2=30V , 0.70V - "0=, T

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
T,	Clock high pulse duration	50			ns	T. PD7-PD0
T.	Clock low pulse duration	50	vol igur		ns	External clock
T.	Clock rise/fall time	8		10		most visieCT.
T.	Chip select setup time	5	No.	STEERE		T. Delay from
T ₂ T ₃ T ₈ T ₉	Chip select hold time	0	yb5h			To Delay from
T ₁₁	IOR* to DDIS* delay		VD.			100 pF load
T ₁₂	Data setup time	15	V03			T Delay from
T ₁₃	Data hold time	15			ns	
T ₁₄	IOW* delay from chip select	10			ns	N Saud rate
T ₁₅	IOW* strobe width	50			ns	
T ₁₆	Chip select hold time from IOW*	0			ns	
T ₁₇	Write cycle delay	55			ns	obus8 = * t s
Tw	Write cycle=T ₁₅ +T ₁₇	105			ns	
T ₁₉	Data hold time	15	ar wall		ns	
T ₂₁	IOR* delay from chip select	10			ns	
T ₂₃	IOR* strobe width	65			ns	
T ₂₄	Chip select hold time from IOR*	0			ns	
T ₂₅	Read cycle delay	55			ns	
Tr	Read cycle=T ₂₃ +T ₂₅	115			ns	
T ₂₆	Delay from IOR* to data			35	ns	100 pF load
T ₂₈	Delay from IOW* to output			50	ns	100 pF load
T ₂₉	Delay to set interrupt from MODEM input			70	ns	100 pF load
T ₃₀	Delay to reset interrupt from IOR*			70	ns	100 pF load
T ₃₁	Delay from stop to set interrupt			1 _{Rclk}	ns	100 pF load
T ₃₂	Delay from IOR* to reset interrupt			200	ns	100 pF load
T ₃₃	Delay from initial INT reset to transmit start	8		24	*	
T ₃₄	Delay from stop to interrupt			100	ns	
T ₃₅	Delay from IOW* to reset interrupt			175	ns	
T ₃₉	ACK* pulse width	75	116		ns	
T ₄₀	PD7 - PD0 setup time	10	CONTRACT OF		ns	

~.}

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified. Sawnorlo assinu 3°0° ± V 0.3=55V 50°0V = *0= T

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
T ₄₁ T ₄₂ T ₄₃ T ₄₄ T ₄₅ T ₄₆	PD7 - PD0 hold time Delay from ACK* low to interrupt low Delay from IOR* to reset interrupt Delay from stop to set RxRdy Delay from IOR* to reset RxRdy Delay from IOW* to set TxRdy	25 5 5		1 _{RCLK}	μS	T, Clock high Clock low Clock low Clock rised Chip select Chip sel
T ₄₇	Delay from start to reset TxRdy Baud rate devisor	1		8	timë ime	T ₁₂ Data setur Data hold T ₁₃ Data hold

Note 1	* = Baudout* cy	cle	0 65		
bac bac	15 15 15 15 15 15 15 15	25 n	105 10 05 0 0 55 115	Write cycle=T _{is} +T _{ir} Data hold time IOR: defay from chip select IOR* strobe width Chip select hold time from IOR* Read cycle delay Read cycle=T _{is} +T _{is} Delay from IOR* to data Delay from IOR* to output	WT WT WT WT WT WT WT WT WT
	100 pF ld pF	70 n 1 _{ee} n 200 n 24 24 100 n 175 n	8 75 10	Delay to set interrupt from MODEM input Delay to reset interrupt from IOR* Celay from stop to set interrupt Delay from IOR* to reset interrupt Delay from initial INT reset to transmit start Delay from stop to interrupt Delay from 1OW* to reset interrupt ACK* puise width PD7 - PD0 setup time	

ABSOLUTE MAXIMUM RATINGS

Supply range
Voltage at any pin
Operating temperature
Storage temperature
Package dissipation

7 Volts GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

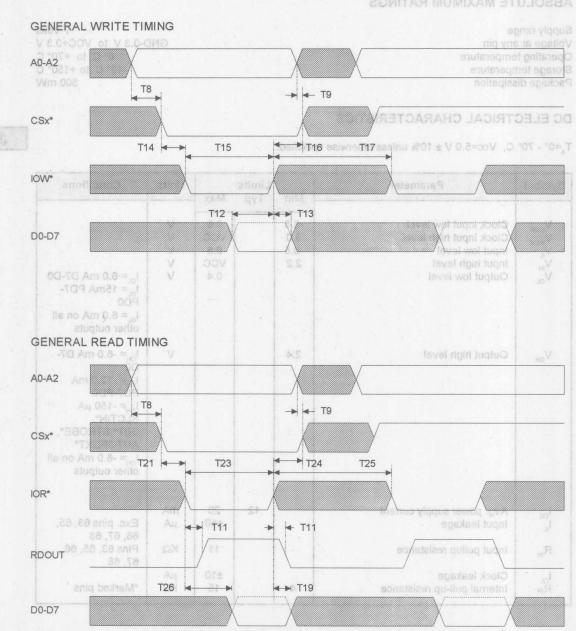
DC ELECTRICAL CHARACTERISTICS

 $T_{A}=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.



Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
V _{ILCK} V _{IHCK} V _{IL}	Clock input low level Clock input high level Input low level	-0.5 3.0 -0.5		0.6 VCC 0.8	V V	70
V _{IH} V _{OL}	Input high level Output low level	2.2		VCC 0.4	V V	I _{ol} = 6.0 mA D7-D0 I _{ol} = 15mA PD7- PD0 I _{ol} = 6.0 mA on all other outputs
V _{OH}	Output high level	2.4			V	I _{OH} = -6.0 mA D7- D0
)(a)					I _{OH} = -12.0 mA PD7-PD0
	\(\alpha\)	et la la				I _{OH} = -150 μA SLCTIN*, INIT*,STROBE*, AUTOFDXT*
	725	711 4		EST		I _{OH} = -6.0 mA on all other outputs
I _{CC}	Avg. power supply current Input leakage	17 *	12	20 ±10	mA μA	Exc. pins 63, 65, 66, 67, 68
R _{IN}	Input pullup resistance			11	ΚΩ	Pins 63, 65, 66, 67, 68
I _{CL} RIN	Clock leakage Internal pull-up resistance	114		±10	μA kΩ	*Marked pins

ABSOLUTE MAXIMUM RATINGS

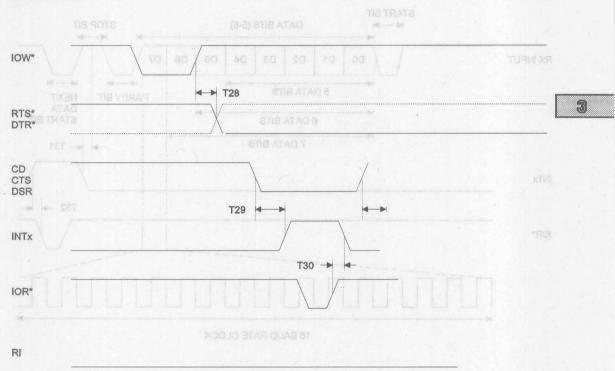


ST16C553

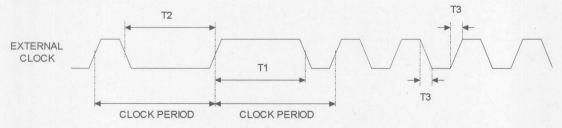
ST16C553

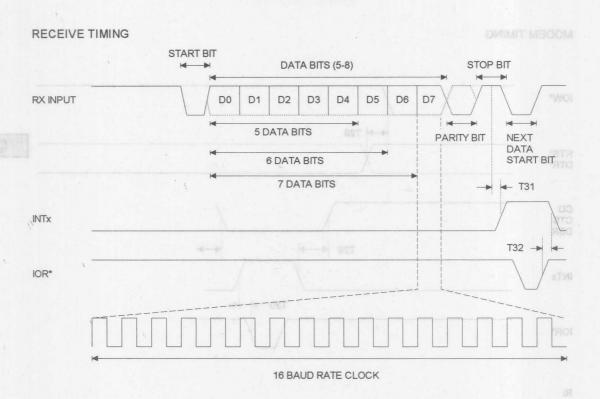


RECEIVE TIMING

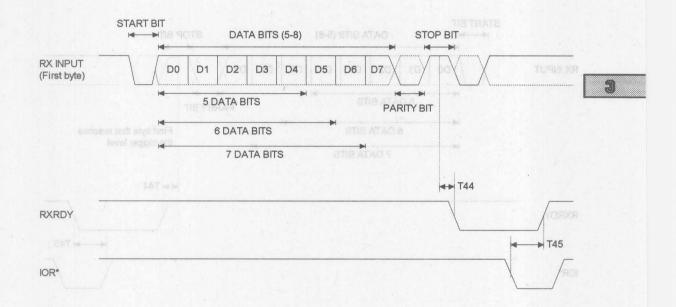


CLOCK TIMING

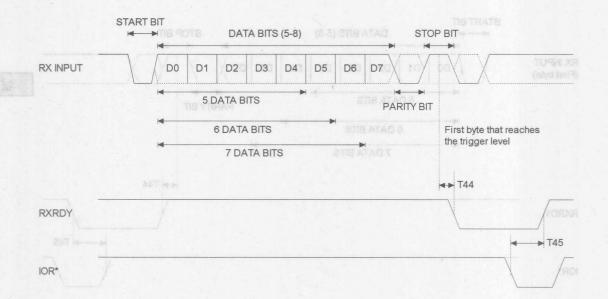


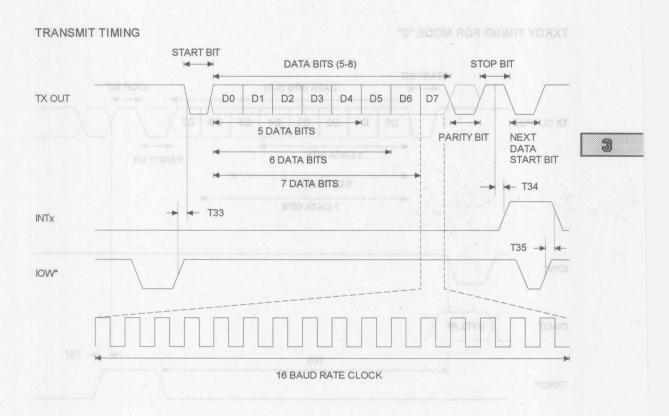


RXRDY TIMING FOR MODE "0"

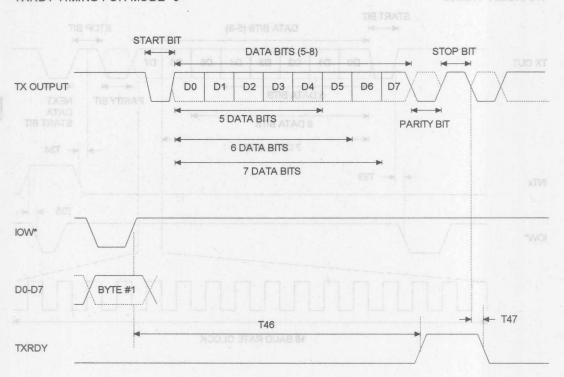


RXRDY TIMING FOR MODE "1"

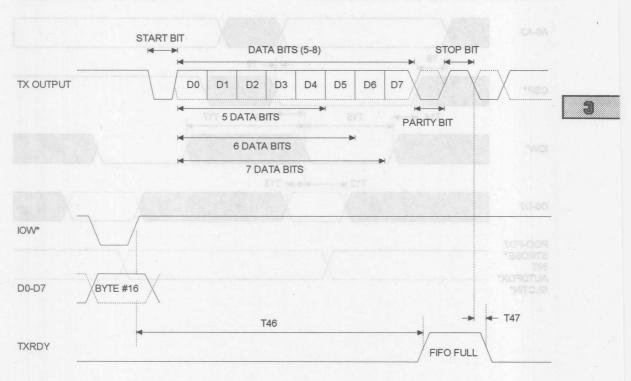


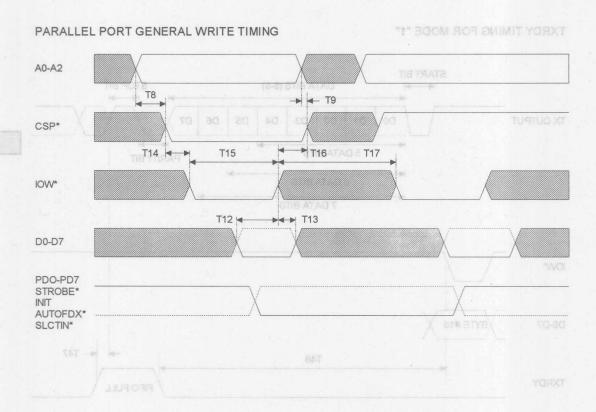


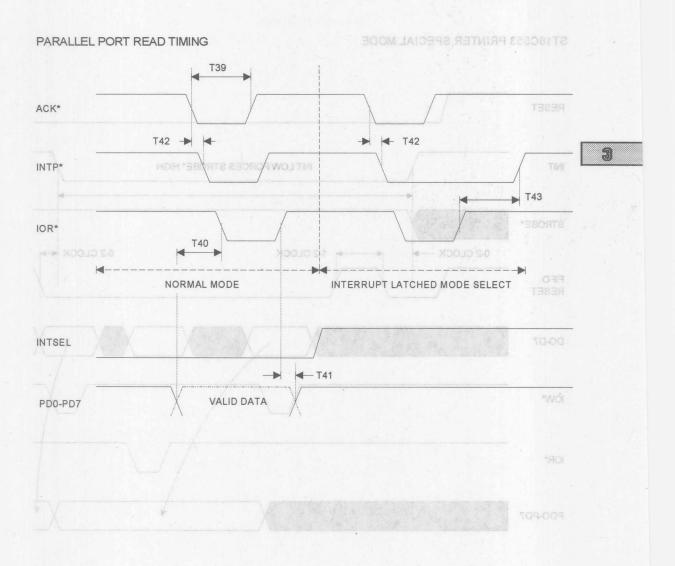
TXRDY TIMING FOR MODE "0"



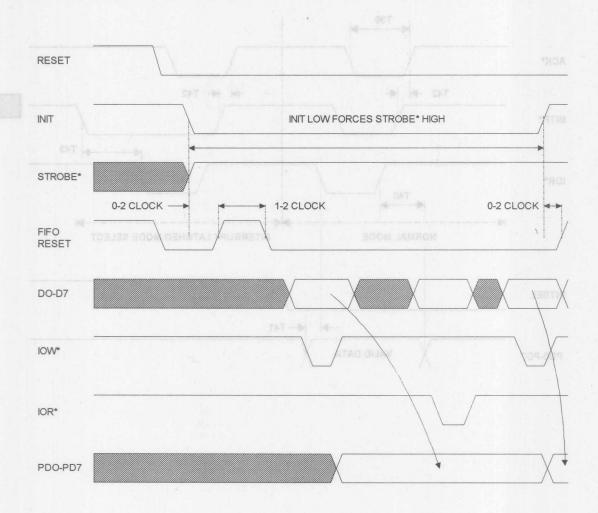
TXRDY TIMING FOR MODE "1"



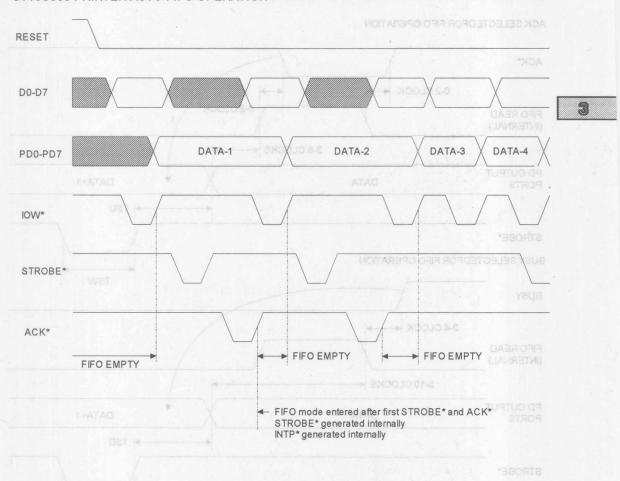




ST16C553 PRINTER SPECIAL MODE

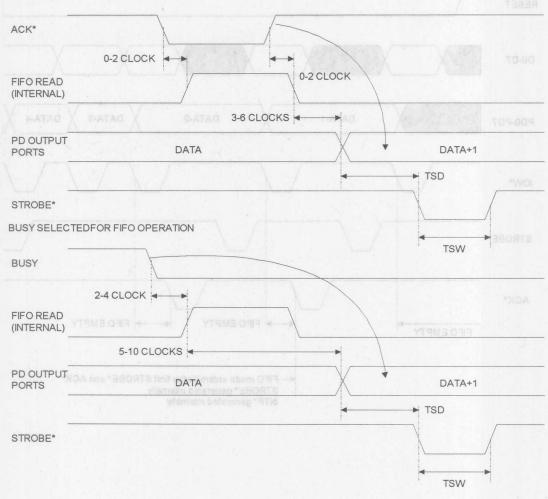


ST16C553 PRINTER AUTO FIFO OPERATION IT BROWN HTM ON HER OFFIRS THIRD ESCONDE



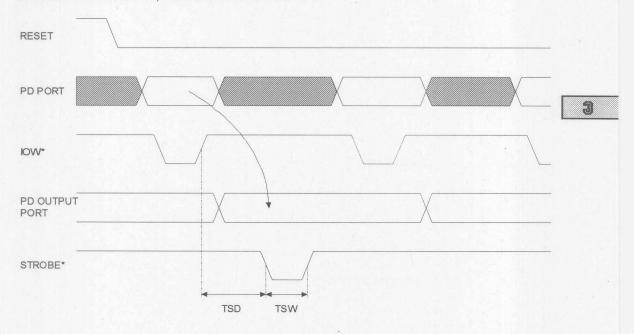
ST16C553 PRINTER FIFO TIMING WITH MORE THAN ONE BYTE IN THE FIFO 1999 55500 TE

ACK SELECTEDFOR FIFO OPERATION

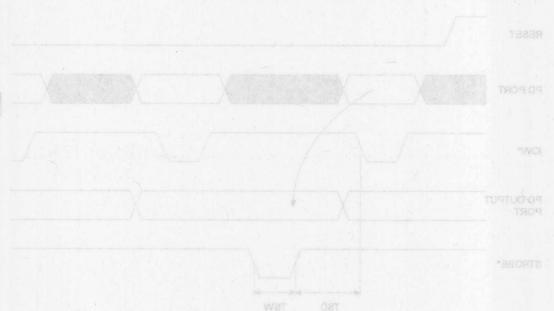


ST16C553

ST16C553 PRINTER FIFO, WITH ONE BYTE IN THE FIFO



STIGOSSS PRINTER FIFO, WITH ONE BYTE IN THE FIFO



Index

PERIPHERALS

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PERIPHERALS	AND TEXT PROPERTY.

Printed September 8, 1994

GENERAL PURPOSE PARALLEL PRINTER PORT WITH 83 BYTE FIFO

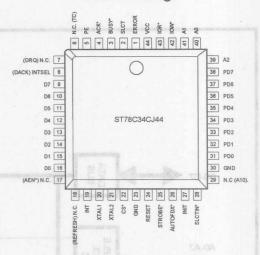
DESCRIPTION

The ST78C34 is a monolithic Bidirectional Parallel port designed to operate as a general purpose I/O port. It contains all the necessary input/output signals to be configured as a CENTRONICS printer port.

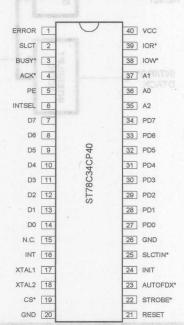
The ST78C34 is a general purpose input/output controller with 83 byte internal FIFO. FIFO operation can be enabled or disabled. For CENTRONICS printer operation, all registers are mapped to IBM printer port registers.

The ST78C34 is designed to operate as normal printer interface without any additional settings. Contents of the FIFO will be cleared after reset or setting the INIT pin to a low state. The auto FIFO operation starts after the first ACK* is received from the printer. Contents of the FIFO transfer to the printer at the printer loading speed.

PLCC Package



Plastic-DIP Package



FEATURES

- 83 bytes of printer output FIFO
- · Bi-directional software parallel port
- Bi-directional I/O ports
- Pin-to-pin compatible to ST78C35
- Register compatible to IBM XT, AT, compatible 386, 486
- · Selectable interrupt polarity
- Selectable FIFO interrupts

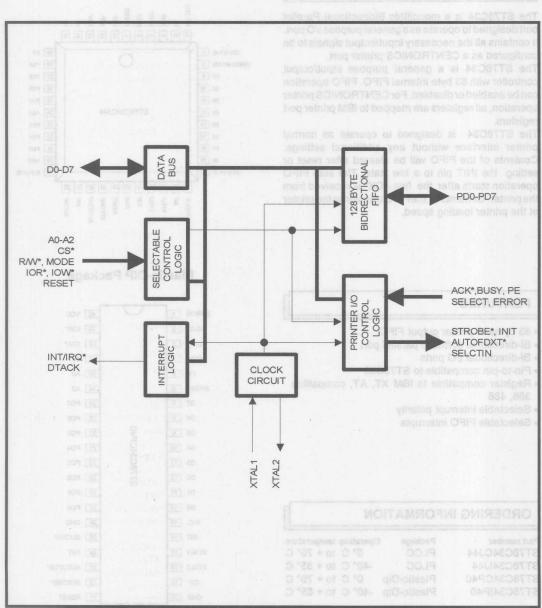
ORDERING INFORMATION

Part number	Package	Operating	temperature
ST78C34CJ44	PLCC	0° C	to + 70° C
ST78C34IJ44	PLCC	-40° C	to + 85° C
ST78C34CP40	Plastic-Dip	0° C	to + 70° C
ST78C34IP40	Plastic-Dip	-40° C	to + 85° C

4

SP 30 L ad 1 Top Cris 181102 18102 1 Fine 18101 1 Vendorate REAL MORE TO

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
ERROR*	1	i power ground.	General purpose input or line printer error (active low). This is an output from the printer to indicate an error by holding it low during error condition.
	high on this piav	et (active high).	RESET 21 I Masterres
SLCT	2 .21	id internal regist	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line
	robe output (ope		printer has been selected.
BUSY	3	ansfer latched d	General purpose input or line printer busy (active high). An output from the printer to indicate printer is not ready to
	e printer auto fe- rinter for continu	urpase I/O or ling. To signal the p	accept data. OV 23 TXGROTUA
	re printer initial a la line printer to	urpose I/O or li h). To signal ti in routine.	low). An output from the printer to indicate that data has
PEtos nimb na	printer 5 slect (an ter	urpose IIO or line slect the line pri	General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.
INTSEL	6	i signal bround.	be selected as an interrupt source by connecting this pin to
	(three state). Totallel port. PD7-P1		the VCC or left open. Connecting this pin to GND will set the interrupt to latched mode, reading the status register resets the INT output.
D0-D7		ne A2 OVI select	transfer information to or from the CPU. D0 is the least
	ernal registers.	nes. To select in	significant bit of the data bus. 78-88
	niq sid15o wol-	oe (active low). If the CPU data	No connect. Should be left open for future expansion.
INT	16	0	Interrupt output (selectable active low or high). To signal the
	Llow level on this 34 data bus to th	ts of the ST78C	state of the printer port. This pin tracks the ACK* input pin, When ACK* is low INT is low and when ACK* is high INT is high if selected as active low interrupt.
VTAL4	47	ply input.	VCC 40 Powersu
XTAL1	17		Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock oscillator circuit.

Symbol	Pin	Signal Type	Pin Description
XTAL2	18	0	Crystal input 2 or buffered clock output. See XTAL1.
CS*		Pin Der	Chip select (active low). A low at this pin enables the ST78C34 / CPU data transfer operation.
GND (wol ovito)		tring a O month	Signal and power ground.
RESET (dgid evilos) but			Master reset (active high). A high on this pin will reset all the outputs and internal registers.
STROBE*	22 grud retning en	peer OVI rated.	General purpose I/O or strobe output (open drain active low). To transfer latched data to the external peripheral or printer.
AUTOFDXT*	23	1/0	General purpose I/O or line printer auto feed (open drain active low). To signal the printer for continuous form feed.
naviedge (a:TINI			General purpose I/O or line printer initialize (open drain active high). To signal the line printer to enter internal initialization routine.
SLCTIN* one			General purpose I/O or line printer select (open drain active low). To select the line printer.
GND XOA Isma			Power and signal ground.
PD7-PD0	34-27	1/O	Bi-directional parallel ports (three state). To transfer data in or out of the ST78C34 parallel port. PD7-PD0 are latched during output mode.
A2 and sales sales			Address line A2. To select internal registers.
A0-A1		termation to or bit of the data	Address lines. To select internal registers.
IOW* seeper s		J. Should be lef	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR* on *AOA s	A nariw boa w	a printat port. The Chief TWI William	Read strobe (active low). A low level on this pin transfers the contents of the ST78C34 data bus to the CPU.
vcc	40	ected as active I I out 1 or external	Power supply input.

PRINTER PORT PROGRAMMING TABLE:

A 1	A0	IOW*	IOR*
0	0	PORT REGISTER	PORT REGISTER
0	1	nalhaen si Jameia pa un	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER
1	1	ALTERNATE FUNCTION REGISTER	FIFO BYTE COUNT REGISTER

^{*} Reading the status register will reset the INT output.

PRINTER FUNCTIONAL DESCRIPTION

The ST78C34 parallel port is designed to operate as a normal CENTRONICS printer interface. The port contains 83 byte FIFO that may be enabled via bit-7 of the Alternate Function Register (AFR). After reset, the FIFO is disabled and the part will function identical to the ST16C552. Once the FIFO is enabled via AFR bit-7, the port will enter FIFO mode after the first byte of data is strobed to the printer and the printer responds with either an ACK* or BUSY signal.

The ST78C34 will remain in FIFO mode until the part is reset or INIT is brought low. While in FIFO mode, data transfer to the printer will be controlled by the printer without any user intervention. The printer port also contains a FIFO byte counter that maintains a count of the number of bytes remaining in the FIFO. The FIFO and the FIFO byte counter are cleared by a reset or by a change of state of the INIT pin. All FIFO related timing is derived from the clock input to pin 17 of the part.

A special parallel port write / read mode is activated when INIT is held low, either by writing a "0" to Control Register bit-2 or by forcing the INIT pin low. In this mode the FIFO read pointer is advanced by reading the parallel port instead of the ACK* or BUSY signals. The STROBE* output is forced high. This allows the user to perform parallel port write and read from operations without strobing data to the printer.

Following an INIT, the parallel port will not be in the

FIFO mode. Control Register bit-0 is used as the STROBE*. Status Register bit-7 is the inverse of the BUSY signal, and INT is derived from ACK*. The transition into FIFO mode will occur after the first STROBE* is generated and the printer responds with either an ACK* or BUSY. In FIFO mode, STROBE* is generated automatically and writing to Control Register bit-0 has no effect on STROBE*. Alternate Function Register bit 0-2 are used to control the delay and width of STROBE*. Handshaking between the printer and the ST78C34 may be controlled by bit-3 of the Alternate Function Register. Setting this bit to a "1" will result in the use of BUSY instead of ACK* for FIFO reading and interrupt control. INT will transition low when a "1" is written to Control Register bit-0 and will transition high when a write to parallel port is performed. In FIFO mode, data transfer to the printer will be controlled by the printer and will occur at the printer's maximum data rate.

The FIFO byte counter is incremented one count for each parallel port write and decremented one count for each FIFO read (data taken by printer). A FIFO read will be generated at the falling edge of either ACK* or BUSY. The byte counter will require two to three clock cycles to update. Hence, a read of FIFO Byte Count Register (FBCR) should only be performed a minimum of three clock after the falling edge of either ACK* or BUSY. The counter is reset whenever the FIFO is reset. If write to parallel port operation is attempted when the FIFO is full, the data



will not be written into the FIFO and the counter will not increment.

Two interrupt modes are available and are selected with the INTSEL pin. If this pin is tied low, a latched interrupt will result. In this mode, INT will transition low when a "1" is written to Control Register bit-0. A reset or reading the Status Register will clear the interrupt. If INTSEL pin is tied high, INT will transition low when a "1" is written to Control Register bit-0 and will transition high when a write to the parallel port is issued. This (non-latched) interrupt signal is always available in Status Register bit-6 regardless of the state of the INTSEL pin. Status Register bit-2 will always contain the latched interrupt state. The polarity of the INT pin may be inverted by setting Alternate Function Register bit-6 high.

The ST78C34 provides additional programmable interrupt output options by programming the Alternate Function Register bit 4-5. INT output can be selected as FIFO full or FIFO empty interrupt.

REGISTER DESCRIPTIONS

PORT REGISTER

Bi-directional printer port.

Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports. Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:

PD7-PD0 bi-directional I/O ports.

STATUS REGISTER IS DOLLAR TO STATUS REGISTER

This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:

This bits are set to "1" normally except when AFR bit 5-4 are both set to "1".

SR BIT-2:

Interrupt condition.

0= an interrupt is pending

This bit will be set to "0" at the falling edge of the ACK* input.

1= no interrupt is pending

Reading the STATUS REGISTER will set this bit to

SR BIT-3:

ERROR input state.

0= ERROR input is in low state

1= ERROR input is in high state

SR BIT-4:

SLCT input state.

0= SLCT input is in low state

1= SLCT input is in high state

SR BIT-5:

PE input state.

0= PE input is in low state

1= PE input is in high state

SR BIT-6:

ACK* input state.

0= ACK* input is in low state

1= ACK* input is in high state

SR BIT-7:

BUSY or FIFO full signal.

0= BUSY input is in high state

1= BUSY input is in low state

FIFO is enabled.

0= FIFO is full

1= One or more empty locations in FIFO

COMMAND REGISTER

The state of the STROBE*, AUTOFDXT*, INIT, SLCTIN* pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0: WAGO TERES JAMESTIXE MORTE

STROBE* input pin.

0= STROBE* pin is in high state
1= STROBE* pin is in low state

COM BIT-1:

AUTOFDXT* input pin.
0= AUTOFDXT* pin is in high state
1= AUTOFDXT* pin is in low state

COM BIT-2:

INIT input pin.

0= INIT pin is in low state

1= INIT pin is in high state

COM BIT-3:

SLCTIN* input pin.

0= SLCTIN* pin is in high state

1= SLCTIN* pin is in low state

COM BIT-4:

Interrupt mask.

0= Interrupt (INT output) is disabled

1= Interrupt (INT output) is enabled

COM BIT 7-5:

Not used. Are set to "1" permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE*, AUTOFDXT*, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:

STROBE* output control bit.

0= STROBE* output is set to high state

1= STROBE* output is set to low state

CON BIT-1:

AUTOFDXT* output control bit.

0= AUTOFDXT* output is set to high state

1= AUTOFDXT* output is set to low state

CON BIT-2:

INIT output control bit.

0= INIT output is set to low state

1= INIT output is set to high state

CON BIT-3:

SLCTIN* output control bit.

0= SLCTIN* output is set to high state

1= SLCTIN* output is set to low state

CON BIT-4:

Interrupt output control bit.

0= INT output is disabled (three state mode)

1= INT output is enabled

CON BIT-5:

I/O select. Direction of the PD7-PD0 can be selected

by setting or clearing this bit.

0= PD7-PD0 are set for output mode

1= PD7-PD0 are set for input mode

CON BIT 7-6:

Not used.

ALTERNATE FUNCTION REGISTER (AFR)

This register En/Disables FIFO operation and provides additional capabilities to control STROBE*. INT and change interrupt functions.

AFR BIT 0-2: and as lamental baldane at

Timing select.

The STROBE* delay and width can be controlled by these bits.

AFR Bit-2	AFR Bit-1	AFR Bit-0	TSD (clocks)	TSW (clocks)
0110	10000	0.010	1 ad 3	00 02 0
11190	0	mu 1 o ad	Totald 5 B. Lon	Pal 0-41 89
1	1	0	1000 5 100 H	18814911
1	1	1	9	8
0	0	0	6	T-14 90
0	0	1	10	8
0	1	0	1009101	8 8
0	1	1	18	16



AFR BIT-3:

Interrupt source.

0= ACK* input pin is selected as printer handshaking source

1= BUSY input pin is selected as printer handshaking source

AFR BIT 4-5: elete doirl of the si tuatuo "VILTOJI2 =0

Interrupt type. State of the INT output pin can be selected for one of the following options.

Bit-5	Bit-4	INT output	SR bit-0	SR bit-6
0	0	Normal mode	1	ACK*
be0 el	en ite se	FIFO empty	o lois	FIFO empty
1	0	FIFO full	p1mg	FIFO full
1	1	FIFO empty	0	FIFO empty
	TV	AND RESIDENCE AND ADDRESS OF THE PARTY OF TH	Second L	

AFR BIT-6:

INT output polarity.

0= Normal. INT output follows the ACK* input

1= Inverted INT output

AFR BIT-7: lorings of selfillideass lengitibbs self-void

FIFO enable / disable function.

0= FIFO is disabled(default mode).

1= FIFO is enabled. Internal 83 byte of FIFO is enabled.

FIFO BYTE COUNT REGISTER (FBCR) and seems

State and content of the printer FIFO can be monitored by reading this register.

FCBR BIT 0-6:

FIFO byte count. Number of characters left in FIFO. FCRB bit-0 is the LSB bit of the counter and FCRB bit-6 is the MSB bit of the counter.

FBCR BIT-7:

FIFO state.

0= FIFO is enabled

1= FIFO is disabled

ST78C34 EXTERNAL RESET CONDITION

SIGNALS	RESET STATE
PD0-PD7 STROBE* AUTOFDXT* INIT	Unknown, output mode High High Low
SLCTIN*	AUTOFDXT* pin is in low shall

AC ELECTRICAL CHARACTERISTICS

ST78C34 REGISTER CONFIGURATIONS

A1	A0	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
0	0	PR	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0 T
0	1	STR	BUSY*/ FIFO full*	None Latched INT	PE 3 0	SLCT	ERROR	Latched INT	loci t rise/ hip selec	1 10
1	0	СОМ		1	100	INT enable	SLCTIN*	INIT	AUTO- FDXT*	STROBE*
1	0	CON	X	X	I/O select	INT mask	SLCTIN*	F TINIT	AUTO- FDXT	STROBE*
1	1	AFR	FIFO	INT polarity	INT type bit-1	INT type bit-0	INT source	TIMING select bit-2	TIMING select bit-1	TIMING select bit-0
1	1	FBCR	FIFO* status	FBC-6	FBC-5	FBC-4	FBC-3	FBC-2	FBC-1	FBC-0

4

AC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Parameter Limits Min Typ Max		Units	Conditions			
T ₁ 009 T ₂ T ₃ T ₈ T ₉	Clock low pulse duration	SLC.	50 50 5 0	PD8 stched stched	10	ns ns ns ns	Exter	nal clock
T ₁₂ T ₁₃ T ₁₄	Data setup time Data hold time IOW* delay from chip select	TM: dàna	15 15 10	1		ns ns ns	CON	
T ₁₅	IOW* strobe width Chip select hold time from IOW* Write cycle delay	INI	50 0 55	X		ns ns ns	(00)	
T ₁₇ Tw T ₃₉ T ₄₀	Write cycle=T ₁₅ +T ₁₇ ACK* pulse width	INT type biled	105 75 10	TWI Vihate	o ald	ns ns ns	AFR	
T ₄₁ T ₄₂ T ₄₃	PD7 - PD0 hold time Delay from ACK* low to interrupt Delay from IOR* to reset interrup		25 5 5	3-08	Or P	ns ns ns	FBC	

ABSOLUTE MAXIMUM RATINGS

Supply range Voltage at any pin Operating temperature Storage temperature Package dissipation 7 Volts GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

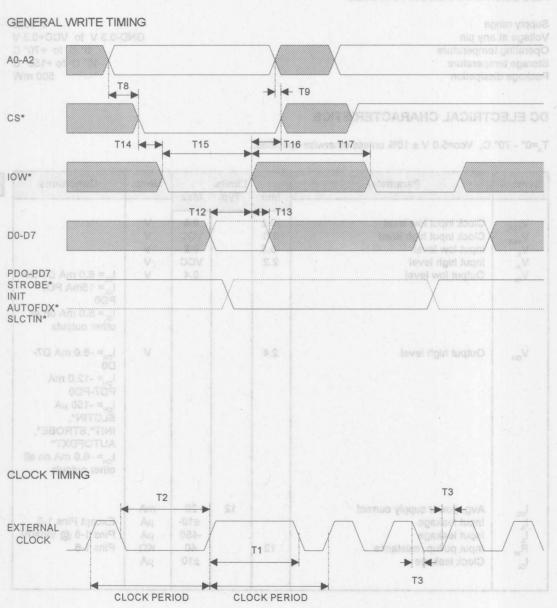
DC ELECTRICAL CHARACTERISTICS

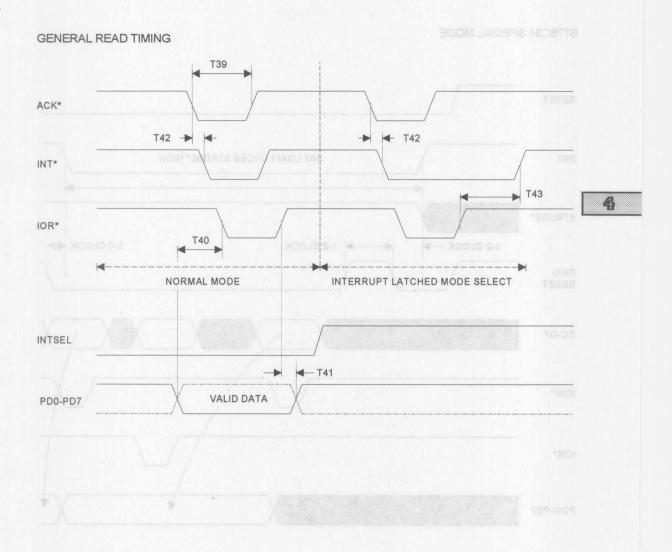
 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

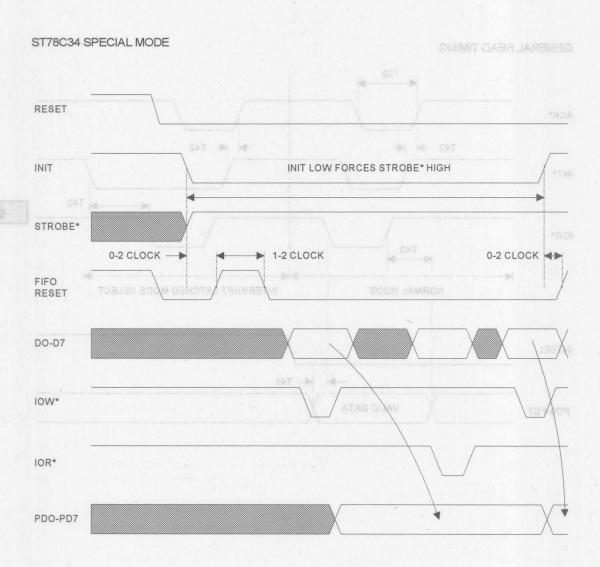
Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
VILCK VIHCK VIL VIH VOL	Clock input low level Clock input high level Input low level Input high level Output low level	-0.5 3.0 -0.5 2.2		0.6 VCC 0.8 VCC 0.4	V V V V	I _{oL} = 6.0 mA D7-D0 I _{oL} = 15mA PD7- PD0
V _{OH}	Output high level	2.4			V	I_{ol} = 6.0 mA on all other outputs I_{oH} = -6.0 mA D7-D0 I_{oH} = -12.0 mA PD7-PD0 I_{oH} = -150 μ A SLCTIN*, INIT*,STROBE*, AUTOFDXT* I_{oH} = -6.0 mA on all other outputs
I _{CC} I _L I _L R _{IN} I _{CL}	Avg. power supply current Input leakage Input leakage Input pullup resistance Clock leakage	12 1	12	20 ±10 -450 40 ±10	mA μA μA ΚΩ μA	Except Pins 1-6 Pins 1-6 @ Vin=0V Pins 1-6

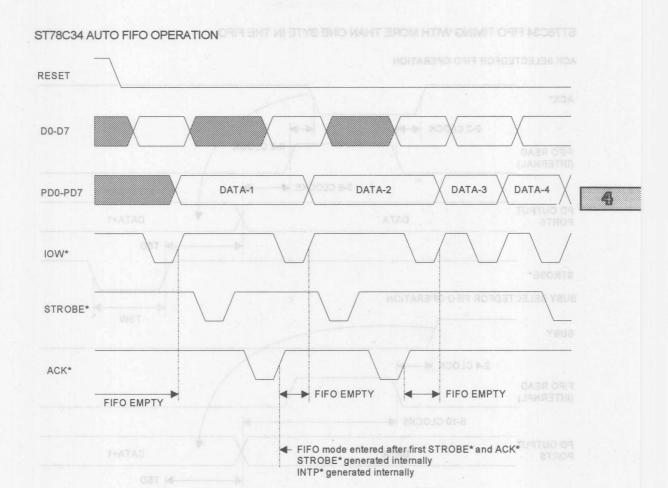
BT - W

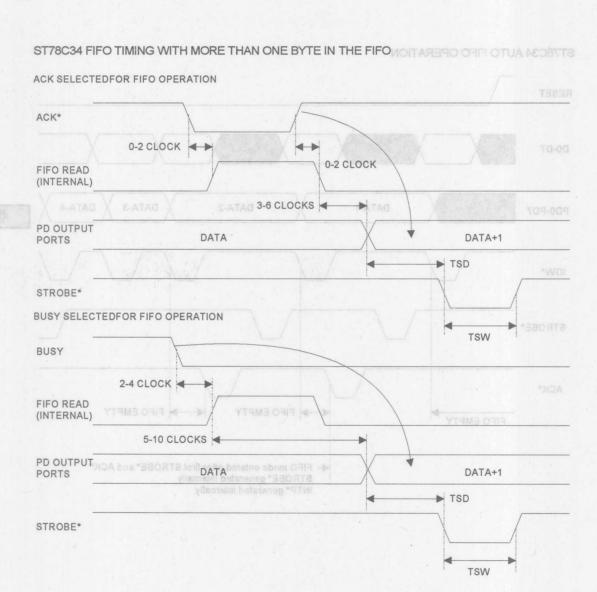
ABSOLUTE MAXIMUM RATINGS



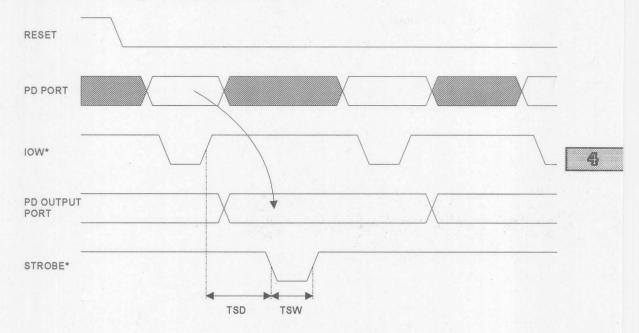






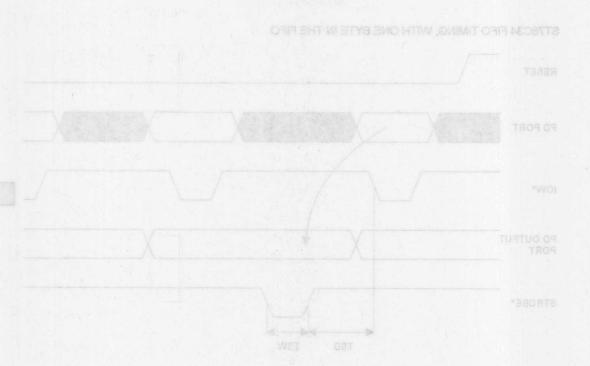


ST78C34 FIFO TIMING, WITH ONE BYTE IN THE FIFO











ST84C01

BOLK <

8 VCC

7 TX

6 IRTX

9 A2 8 A1

5 RESET

4

Printed September 7, 1994

INFRARED RECEIVER AND TRANSMITTER

DESCRIPTION

The ST84C01/02 is a single channel Infrared receiver and transmitter, designed for wireless peripheral communications. It meets the standard IrDa specification for wireless applications. The ST84C01 is offered with standard and programmable custom frequencies. The ST84C01 can interface directly to ST16C450, ST16C550, and ST16C650 products.

ST84C01/02 is designed in a 1.2µ process to achieve 115.2k baud transmission rate.

Plastic-DIP Package

8 VCC 16XBAUD 1 ST84C01CF8 7 TX RX 2 6 IRTX IRRX 3 GND 4 5 RESET

ST84C02CF8

EXCLK 1

RX 2

IRRX 3

GND 4

GND 6

A0 7

FEATURES

- Selectable transmit/receive bit rate
- . 8, 14 pin DIP or SOIC package.
- · Crystal oscillator circuit on board

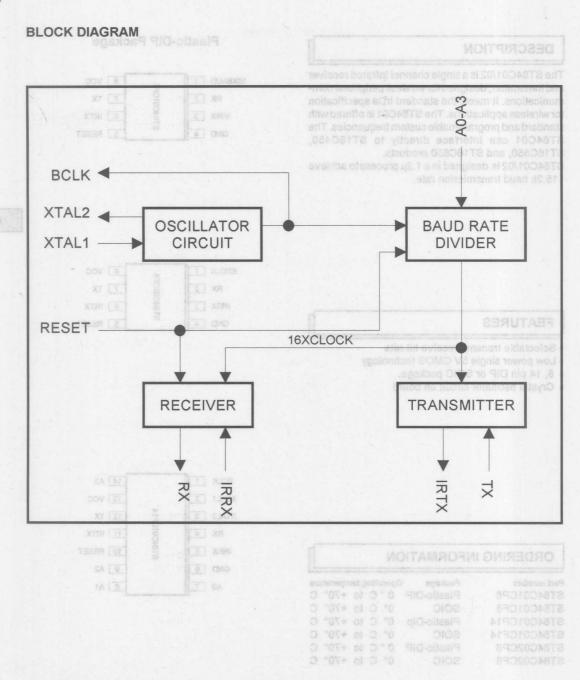
Low power single 5V CMOS technology

14 A3 BCLK 1 XTAL1 2 13 VCC ST84C01CF14 XTAL2 3 12 TX RX 4 11 IRTX 10 RESET IRRX 5

ORDERING INFORMATION

Part number	Package	Operating	temperature
ST84C01CP8	Plastic-DIP	0°C	to +70° C
ST84C01CF8	SOIC	0° C	to +70° C
ST84C01CP14	Plastic-Dip	0° C	to +70° C
ST84C01CF14	SOIC	0° C	to +70° C
ST84C02CP8	Plastic-DIP	0°C	to +70° C
ST84C02CF8	SOIC	0° C	to +70° C

INFRARED RECEIVER AND TRANSMITTER



SYMBOL DESCRIPTION (ST84C01CP/CF14 Package) MONTHINGE OF LOSMYS

Symbol	Pin	Signal Type	Pin Description
BCLK		2 rate Olok Input.	Buffered clock output. To drive external UART clock.
XTAL1	2 rd UART data	taretos, This pin out pin I ata output. Standa with 1 start and s	Crystal or External Clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal reference
XTAL2	3	0	Crystal clock output.
RX	4	ceive data input O	Receive data output. Standard UART data output for 8 bits
IRRX	metni lesen o	at (active high). The transmitter.	Infrared receive data input.
		ansmit One output	
A0	7*	word with t star	Address select 0. To select the internal preprogrammed data rates.
A1		lata input. Standa with 1 Mart and st	
A2	9*	apply Input.	Address select 2. To select the internal preprogrammed data rates.
RESET	10	1	Reset input (active high). To reset internal counters, receiver and transmitter.
IRTX	11	0	Infrared transmit data output. Converted standard UART 8 bits wide word with 1 start and stop bit to IrDa specified pattern.
TX	12	1	Transmit data input. Standard UART data input for 8 bits wide word with 1 start and stop bits.
vcc	13	1	Positive supply input.
A3	14*	L	Address select 3. To select the internal preprogrammed data rates.

^{*} Have internal pull-up resistors



SYMBOL DESCRIPTION (ST84C01CP/CF8 Package) DASTE) MOITGIFFORED LOBMYS

Symbol	Pin	Signal Type		Pin Des	cription	
an be connected larnal reference	ut. A crystal cr o generate in licati 2 1, XTAI	lock output. To din External Clock In pl and XTAL2 pin to extern O clock app affered clock output	receive data 550 baud-ou Receive dat	rates. This pin ut pin. a output. Stand	nt. User selectab can be connected dard UART data stop bits conve	d to ST16C450/
			receive data	1.		
IRRX	3	ck output	The second second second	eive data input		
		eta outpat. Sianda	Receive d	0	4	
GND mont bene	op bi 4 s recov	with 1 O art and st	Supply grou	nd.		
RESET	5	ceive data input.	Reset input		To reset interna	al counters, re-
TX	7	elect 1. To select	bits wide wo pattern. Transmit da	ord with 1 star ta input. Stand with 1 start and	ut. Converted state and stop bit to dard UART data stop bits.	IrDa specified
bonins gorgan	ismotni orb	tobles of S toble	1 OSILIVE Sup	pry mpat.	*0	SA
			data rates			
ial counters, re-	o reset intern	ut (active high). T I transmitter.			10	
	and stop bit i	ensmit data output word with 1 start o		0	11	хтя
	rd UART data		bits wide pattern.	0	11	
	rd UART data	word with 1 start of	bits wide pattern. Transmit o	0		IRTX

SYMBOL DESCRIPTION (ST84C02CP/CF8 Package)

Symbol	Pin	Signal Type	Pin Description
EXCLK	1	ı	1.8432 MHz clock input. For custom data rates, see the data rate selection table.
RX	2	0	Receive data output. Standard UART data output for 8 bits wide word with 1 start and stop bits converted from IRRX receive data.
IRRX DISTOR	3 Haru	l _{effort2}	Infrared receive data input.
GND	4	0 0	Supply ground.
Am 0.8 = .01	5 ∨	0.6	Reset input (active high). To reset internal counters, receiver and transmitter.
Pin s only XTSI VINE Voc Pin 3 No had	8 Au Au Am	0 -100 1 1,2 1,2 60 85	Infrared transmit data output. Converted standard UART 8 bits wide word with 1 start and stop bit to IrDa specified pattern.
TX	7	- I 00	Transmit data input. Standard UART data input for 8 bits wide word with 1 start and stop bits.
vcc	8	1	Positive supply input.

DATA RATE SELECTION TABLE

А3	A2	A1	A0	BAUD RATE	DIVISOR
0	1	0	1	600	192
0	1	1	0	1200	96
0	1	1	1	2400	48
1	0	0	0	3600	32
1	0	0	1	4800	24
1	0	1	0	7200	16
1	0	1	1	9600	12
1	1	0	0	19.2k	6
1	1	0	1	38.4k	3
1	1	1	0	57.6k	2
1	1	1	1	115.2k	1



ABSOLUTE MAXIMUM RATINGS (speaks 9 870/9000 ABT 2) MORTHINGS (Speaks 9 870/900 ABT

Supply range		7 Volts
Voltage at any pin		GND-0.3 V to VCC+0.3 V
Operating temperature	and the same of the same of the same of	0° C to +70° C
Storage temperature		-40° C to +150° C
Package dissipation		500 mW

DC ELECTRICAL CHARACTERISTICS

 T_{Δ} =0 - 70° C, VCC=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
	y ground.		-21			GND
V _{IL}	Input low level			0.8	V	
unter V re-	Input high level T (1911 evilps) fugni	2.0	1		V 3	RESET
V _{oL}	Output low level	seiver		0.5	V	I _{oL} = 6.0 mA
V _{OH}	Output high level	2.8			V	I _{OH} = 6.0 mA
B TIRAU b	Input low current Judiuo also limaned by	Infran	0	-100	μА	Pin 3 only
specified	Input high current	bits w		1	μА	V _{IN} =Vcc Pin 3
A 1	Operating current		1	1.2	mA	No load.
R _{IN}	Input pull-up resistance	35	50	65	ΚΩ	
etid 8 not	nit data input. Standard UART data input		1			XT

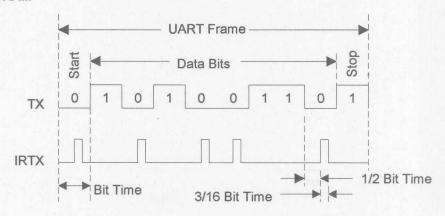
AC ELECTRICAL CHARACTERISTICS

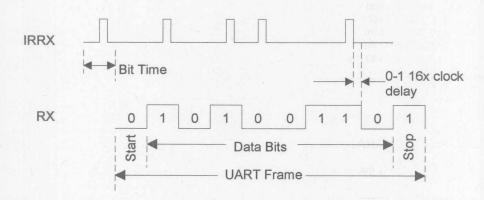
 $T_A=0-70^{\circ}$ C, VCC=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
T ₁ T ₂	CLOCK rise time CLOCK fall time		1.5 1.5	2 2	ns ns	0.5V - 2.8V 2.8V - 0.5V
				16	7200	0 1 0 1

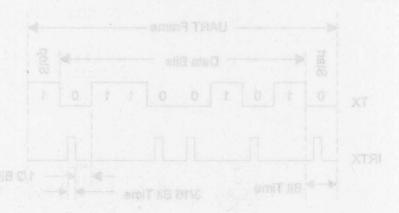
4

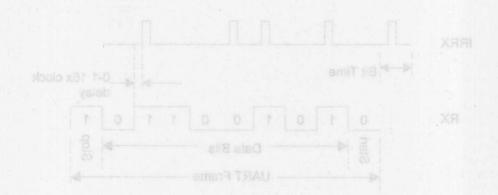
TIMING DIAGRAM





THINING DIAGRAM







ST84C72

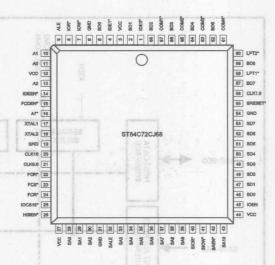
Printed September 7, 1994

IDE INTERFACE WITH I/O DECODE

DESCRIPTION

The ST84C72 is designed to replace all necessary TTL logics for 16 bit IDE interface and decode logic for floppy controller and serial / parallel I/O ports. A select pin is provided to select primary or secondary address for hard and floppy decodes. On board crystal oscillator circuit provides 16, 9, and 1.8461 MHz clock outputs for some floppy controllers and uart from 48 MHz external crystal connected to ST84C72.

PLCC package



FEATURES

- · Low power CMOS design
- Direct bus connect
- Replacement for more than 7 TTL parts
- · High speed for new design
- Selectable I/O decode ports. (COM1-COM4, LPT1-LPT2)
- · Floppy address decode
- Pin selectable primary and secondary address decodes

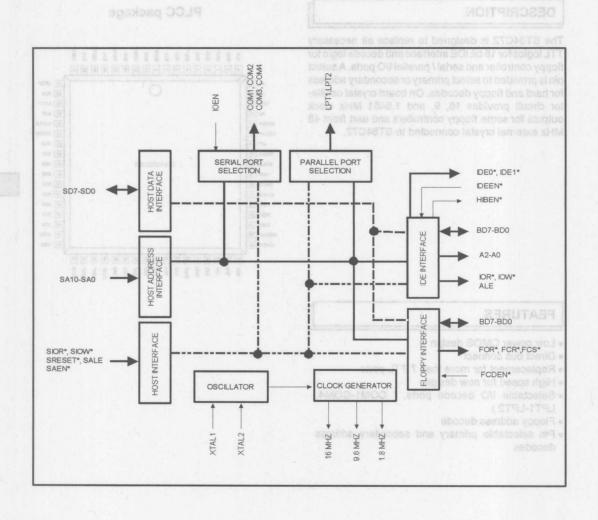
ORDERING INFORMATION

Part number ST84C72CJ68 Package PLCC Operating temperature 0 ° C to +70 ° C 4

STARTECH

IDE INTERPACE WITH ITO DECODE

BLOCK DIAGRAM



Symbol	Pin	Signal Type	Pin Description
SA0-SA2	28-30	mmunidation sele	Host address lines A0-A2.
SA3-SA9	33-40	(1-MOO) x5	Host address lines A3-A9.
SA10	43	nntunication sele ex (COM-2).	Host address line A10.
SALE	evilo 32 lq to	nmunichtion sele	Host address latch enable (active high).
SAEN* beboodd .(wo	42 evilos) nig to		Host address enable (active low). All decoded addresses are valid when SAEN* is low.
a by 28). This	41 mail clock divid	equency or exter	Host I/O write signal input (active low). Buffered data bus (BD7-BD0) are gated with SIOW*, SIOR* and I/O decoded addresses to insure proper valid data time slots.
SIOR*	04 oss Connectin	cation dock. Learning port acts JT) of the ST16C4	Host I/O read signal input (active low).Buffered data bus (B07-BD7) are gated with SIOR*, SIOW* and I/O decoded addresses to insure proper valid data time slots.
SD0-SD7	46-53	1/0	Host data bus.
SRESET*	55 emetri) eldezi nerw beldselb	orts are not used introller enabled introller salect it	Host system reset (internally pulled up, active low). This pin is used to set internal clock dividers to known state. For normal operation this pin should be left open or connected to VCC.
nost SA PLATX and 3F2 Hox) tany selection	conn.71 ed fo 3F7, 3F5, 3F4 3F2/2 (secon 372 Hax)	tput pin of the \$1 77, 375, 374 and	Crystal or external clock input. A crystal can be connected between XTAL1 and XTAL2 with some additional filters to generate 48 Mhz clock frequency for floppy controller and UART clock. This pin can be connected to VCC or GND if CLK16, CLK9.6 and CLK1.8 are not used.
XTAL2	18	ntroller address o O ntroller address o	Crystal output. This pin should be left open if external clock is used to connect to XTAL1 or clock is not used.
LPT1*oH 8-4-78	58 000	atrolle O ddress	Line printer enable (active low). Primary printer enable signal. Decoded for address 378 Hex (LPT1).
		lock output gare	Line printer enable (active low). Secondary printer enable signal. Decoded for address 278 Hex (LPT2).

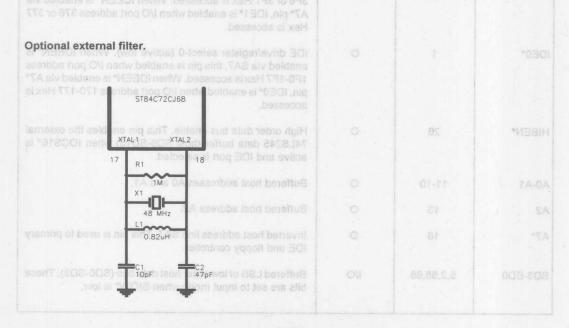


Symbol	Pin	Signal Type	Pin Description
COM1*	67	ess lino AD-A2.	Serial communication select pin (active low). Decoded for 3F8 Hex (COM-1).
		ess lines A3-A9.	
COM2*	65	ess tine A10.	Serial communication select pin (active low). Decoded for 2F8 Hex (COM-2).
COM3*			Serial communication select pin (active low). Decoded for 3E8 Hex (COM-3).
	ze low). All deco		
COM4*		then SOEN* is I	Serial communication select pin (active low). Decoded for 2E8 Hex (COM-4).
	(active low). But		
slots. fered data bus	StOW95*10R* a valid data time (active tow). But SIOR*, SIOW* a	to insure properadoral input	1.8461 Mhz clock output generated from 48 Mhz crystal (crystal frequency or external clock divide by 26). This clock can substitute the standard 1.8432 Mhz serial communication clock.
slots. NaOl	valid 24 to time by pulled up, activated to to	to insure prope bus. m reset (internat	Serial and parallel port access. Connecting this pin to pin 44 (RDOUT) of the ST16C452, ST16C552, or ST16C553 enables the BD0-BD7 to access the serial and parallel ports. This pin should be tied to GND if external serial/parallel ports are not used.
n or *Madda n be connected filters to a controller and	hould 21 left ope put. A crystal ca 2 with some add quency for floop be connected to 8 are not used.	eration this pin a extental clock in TAL1 and XTAL 8 Mhz clock fre ck. This pin can	
FOR*	22 nego led ed blue	0	Floppy controller address decode (372/3F2 Hex).
			Floppy controller address decode (377/3F7 Hex).
FCR* relining	78mir 24 vol e	encole (activ	Floppy controller address decode (374-5/3F4-5 Hex).
CLK16	20	o r enable (active	16 Mhz clock output generated from 48 Mhz crystal (crystal frequency or external clock divided by 3).

Symbol	Pin	Signal Type	Pin Description
	al W/(21) nadw		9.6 Mhz clock output generated from 48 Mhz crystal (crystal frequency or external clock divide by 5).
IOCS16*	BD7 is set to in	read operation low.	IDE 16 bit data transfer enable (internally pulled up, active low). This pin enables the external 74LS245 bus driver (HIBEN*) when IDE port is selected and 16 bit data transfer is required.
IDEEN*	14 nal (HIOR*).	iost address late lost I/O read sig lost I/O write sig f power ground.	IDE Enable/Disable (internally pulled up). IDE select is disabled when this pin is left open or connected to VCC. IDE controller can be selected when this pin is connected to A7* output pin of the ST84C72 (primary selection address 3F0-3F7 and 1F0-1F7 Hex) or host address line SA7 (secondary
IDE1*	4	Onlygo	IDE drive/register select-1 (active low). When IDEEN* is enabled via SA7, this pin is enabled when I/O port address 3F6 or 3F7 Hex is accessed. When IDEEN* is enabled via A7* pin, IDE1* is enabled when I/O port address 376 or 377 Hex is accessed.
IDE0*	1	0	IDE drive/register select-0 (active low). When IDEEN* is enabled via SA7, this pin is enabled when I/O port address 1F0-1F7 Hex is accessed. When IDEEN* is enabled via A7* pin, IDE0* is enabled when I/O port address 170-177 Hex is accessed.
HIBEN*	26	0	High order data bus enable. This pin enables the external 74LS245 data buffer (host SD8-SD15) when IOCS16* is active and IDE port is selected.
A0-A1	11-10	0	Buffered host addresses A0 and A1.
A2	13	0	Buffered host address A2.
A7*	16	0	Inverted host address line SA7. This pin is used to primary IDE and floppy controller.
BD3-BD0	5,2,68,66	1/0	Buffered LSB of low order host data bus (SD0-SD3). These bits are set to input mode when SIOW* is low.

4

Symbol	Pin	Signal Type	Pin Description
BD4-BD6		ON cok output gener	
245 bus driver	77 able (internally p a external 74LS	OVI data transfer en pin enables th when IDE port is	Buffered host data bit -7 (SD7). This bit goes to high impedance when address 3F7 or 1F7 Hex is accessed during I/O read operation. BD7 is set to input mode when SIOW* is low.
ALE	9	0	Buffered host address latch (SALE).
IOR*DOV of bei	open 8 connec		Buffered host I/O read signal (HIOR*).
IOW*anibbs no	(primar 7 selecti		Buffered host I/O write signal (HIOW*).
		F0-1F7 Hex) or laddres 0 70-37	Signal and power ground.
Inen IDE COOV	3,12,27,44	/registel select-	Power supply input. *130



ABSOLUTE MAXIMUM RATINGS

Supply range Voltage at any pin Operating temperature Storage temperature Package dissipation 7 Volts GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

DC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter		imits Typ Max	Units	Conditions
VILCK	Clock input low level	-0.5	0.6	V	
VIHCK	Clock input high level	3.0	VCC	V	
V _{II}	Input low level	-0.5	0.8	V	
V _{IL} V _{IH}	Input high level	2.2	VCC	V	
V	Output low level on all outputs		0.4	V	I _{oL} = 6 mA
V _{OL} V _{OH}	Output high level	2.4		V	I _{OH} = -6 mA
Icc	Avg power supply current		15	mA	On
I	Input leakage		±10	μΑ	
ICL	Clock leakage		±10	μA	



ABSOLUTE MAXIMUM RATINGS

Supply range Voltage at any pin Operafing temperature Storage temperature Package dissipation

7 Volts
0° C to +70° C
40° C to +150° C
500 mW

DC ELECTRICAL CHARACTERISTICS

T.=0° - 70° C. Vcc=5.0 V ± 10% unless otherwise specified.

Am 8 = 6 V V V V V V Am 8- = 6 V Am Au	2.05 2.05 2.2 2.2 2.4	Clock input tow level Clock input high level Input fow level Input high level Output high level on all outputs Output high level Avg power supply current Input leakage Clock leakage	

Printed September 7, 1994

FLOPPY DISK SUBSYSTEM CONTROLLER

DESCRIPTION

The ST37C65 Floppy Disk Subsystem Controller is an LSI device that provides all the needed functionality between the host processor and the floppy disk drive. This "super-chip" integrates the following functions: formatter / controller, data separation, write precompensation, data rate selection (to a maximum of 1Mbit per second), and clock generation. It also provides interface drivers and receivers for the floppy

The ST37C65 is functionally compatible pin-for-pin with the WD37C65C. In addition the ST37C65 Supports a power down mode for laptop and portable systems.

FEATURES

- IBM*PC AT* compatible format (single and double density)
- · BIOS compatible, supports dual speed spindle
- · Address mark detection circuitry (internal to floppy disk controller)
- · Multi-sector and multi-track transfer capability
- · Direct floppy disk drive interface (no buffers needed)
- · 48 mA sink output drivers
- · Automatic write pre-compensation Disable option, Pin selectable inner track values of 125 or 187 nanoseconds
- Integrated high-performance DPLL data separator, industry standard error rates of <10E-9
- Data rates of 125, 250, 300, 500 Kbits/second and 1 Mbit/second
- · User programmable track stepping rate and head load/unload times
- · Supports four floppy drives

ORDERING INFORMATION

Part number ST37C65CJ44 ST37C65CP40 **Package PLCC**

Operating temperature 0° C to + 70° C Plastic-Dip

0° C to + 70° C

PLCC Package



DIP Package

RD*	1		40 VCC
WR*	2		39 IDX*
CS*	3	DISTRIBUTED SEED	38 TR00*
A0	4		37 WP*
DACK*	5		36 RWC*/RPM*
тс	6		35 HDL*
D0	7		34 MO2* /DS4*
D1	8		33 MO1*/DS3*
D2	9	40	32 DS2*
D3	10	ST37C65CP40	31 GND
.D4	11	208	30 DS1*
D5	12	ST3	29 STEP*
D6	13		28 DIRC*
D7	14		27 WD*
DMA	15		26 WE*
IRQ	16		25 HS*
LDOR*	17		24 PCVAL
LDCR*	18		23 CLK1
RST	19		22 DRV
RDD*	20		21 CLK2

LOPPY DISK SUBSYSTEM CONTROLLER

BLOCK DIAGRAM

CONTROL MASTER STATUS REGISTER OPERATION REGISTER D0-D7 CLOCK AND TIMING GENERATOR ALU DMA,IRQ INSTRUCTION HOST DECODE HS*,HDL*,STEP* DIRC*,RWC* DS1*-DS4* RD*,WR*,CS* A0,DACK*,TC PROGRAM DISK LDCR*LDOR* MS TIMER STATE MACHINE A TR00*,IDX* WP*.DCHG* FLAG RDD* WE* PCVAL WRITE PRE-COMPENSATION CRC GENERATOR tor, industry standard error rates of <105-9

Symbol	Pin	Signal Type	Pin Description
		recial AT/EISA	
		DMAEN signal fr	Read signal (active low). Control signal for transfer of data or status onto the data bus by the ST37C65.
		eEnable (active)	CHGEN* 17 DiskChang
WR*becking ed	atus at 2 in 40 to RO" of LDCR*.	e DCHCP linguit st data bus during	Write signal (active low). Control signal for latching data from the bus into the ST37C65 buffer register.
		I itions Register I es the loading of	Chip select (active low). Selected when low allowing RD* or WR* operation from the host.
	the stable whi	with WH* create a the Operations	Address line 1. Address line selecting data or status information.
emally gated		of Register (activities of the Compart the Compart the Strobews into the Control	DMA ACKNOWLEDGE (active low). Used by DMA controller to transfer data from the ST37C65 onto the bus. AT/EISA mode, this signal is qualified by DMAEN from the Operation Register.
s Putsdevice		tive hlgh). B ncertn idle, Rese de, not PC AT o data. This is the	ST37C65 that data transfer is complete. If DMA operation mode is selected for command execution, TC will be qualified by DACK*, but not in the programmed I/O execution. In AT/EISA or Special mode, qualification by DACK*
		ach falling edge encoded data.	requires the Operation Register signal DMAEN to be logi- cally true. Note also AT/EISA mode, TC will be qualified by DACK*, whether in DMA or non-DMA host operation. Pro-
		r, level glock ing MHz for 300 kb/s Register.	grammed I/O in AT/EISA mode will cause an abnormal termination error at the completion of a command.
DB0-DB7	7-14	1/0	Data bus. 8 bit, bi-directional, three state, data bus. DB0 id
liator is con-	it. A crystal osc	flator drive outp	the least significant bit and DB7 is the most significant bit.
		this pin to XTA	Toll Beigen
DMA Used for non-		TL InprO used a ligher or Externa ta rates.	Direct Memory Access (three state, active high). DMA request for byte transfers of data. In Special or AT/EISA mode, this pin is three stated, enabled by the DMAEN signal from the Operation Register. This pin is driven in the Base mode.
ow that a two		This inout indic	NRV 24 I Drive Type
IRQ sees had	16 00 1	lle mot O is used ok input will ner	Interrupt (three state, active high). Interrupt request indicating the completion of command execution or data transfer requests (in non-DMA mode). Normally driven in Base



Symbol	Pin	Signal Type	Pin Description
		(active low). Cont	mode. In Special AT/EISA mode, this pin is three stated, enabled by DMAEN signal from the Operation Register.
DCHGEN* steb grinbtel	17 not signal for sign reflud 3	I (active low), Con sinto the ST3706	Disk Change Enable (active low). This input must be at logic "0" to enable DCHG* input status at pin 40 to be placed on bit-7 of the data bus during RD* of LDCR*. It has internal pull-up.
LDOR*	18	active low). Selection from the host. 1 Address fine s	
bus AT/EISA		OWLED BE (act v rdata from the ST goal is qualified by	
MA operation r, TC will be		ount (alctive Ingle at data transfer's lected for comm	Reset (active high). Resets controller, placing microsequencer in idle. Resets device outputs. Puts device in Base mode, not PC AT or Special mode.
on by DA*DDA EN to be logi- te qualified by	ode, 12 alificates signal DMA mode, TC will	DACK*, but not a EISA or Especial m Operation Regist ore also AT/EISA	Read Disk Data. This is the raw serial bit stream from the disk drive. Each falling edge of the pulses represents a flux transition of encoded data.
*CLK2 nds ns	ode v12 cause letion of a con	ather in DMA or so O in AT/EISA in error at the comp	Clock-2. TTL level clock input used for non-standard data rates; is 9.6 MHz for 300 kb/s, and can only be selected from the Control Register.
XTAL20 offings	teom (22 at 18	bit, &l-directions, milicanOsit and Di nory Access (thre	Crystal oscillator drive output. A crystal oscillator is connected from this pin to XTAL2i pin. This pin should be left floating if TTL inputs used at pin XTAL2i.
XTAL2i	23 3	byte transfers of in is thut estated in eration Register.	Crystal oscillator or External clock input pin. Used for non-
data transfer		I ree state, active si pletion of comma n non-DMA mode	Drive Type. This input indicates to the device that a two speed spindle motor is used if logic is "0". In that case, the

Symbol	Pin	Signal Type	Pin Description
*CLK1	23	nd.	Clock1. TTL level clock input is used to generate all internal timing for standard data rates. Frequency must be 16 MHz $\pm 0.1\%$ or 32 MHz $\pm 0.1\%$, and may have 40/60 or 60/40 duty cycle.
XTAL10	from 25 Opera se, this output is	nis sig of corner e, er Special mod it Selects, as app	Crystal oscillator drive output. A crystal oscillator is connected from this pin to XTAL1i pin. This pin should be left floating if TTL inputs used at pin XTAL1i.
se mode, or decoded Unit	Register. In Ba #3 of the four	able for disk dri the Operation le, this output is specified in the d	Crystal oscillator or External clock input pin. Requires 16 MHz or 32 MHz crystal. This oscillator is used for all standard data rates, and may be driven with TTL level signal.
PCVAL (i). This signal se mode, or teccoded Unit	e #2 (active low Register. In Ba #4 of the four	able for disk driving the Operation let this output is specified in the contract of the contra	Pre-Compensation Value. This pin determines the amount of write pre-compensation used on the inner tracks of the diskette. Logic "1" = 125 ns, logic "0" = 187 ns. If the data defeat option is used, PCVAL is unimportant and pre-compensation is disabled.
drive.		active (o). When againt the med	Head Select (active low). High current driver (HCD) output selects the head (side) of the floppy disk that is being read or written. Logic "1" = side 0.
rent when *aW s, becoming	ducedegrite Cultine inner traci	low, ceores a Resortación de la Resortación de l	Write Enable (active low). The output becomes true, just prior to writing on the diskette. This allows current to flow through the write head.
	TENTA 30 HI VO	sation onecass active when C	Write Data. Each falling edge of the encoded data pulse stream causes a flux transition on the media.
en or that the	t drive door is o	(activoow). The	Direction (active low). DIRC* determines the direction of the head stepper motor. Logic "1" = outward motion.
STEP*	since the lest di 32 This input sense	O flug to	Step Pulse (active low). STEP* output issues an active low pulse for each track to track movement of the hrad.
DS1*	elb is 133 w wo	ndeallo active	Drive Select-1 (active low). It enables the interface to this disk drive. This signal comes from the Operation Register. In Base mode, or Special mode, this output is #1 of the four decoded Unit Selects, as specified in the device command



Symbol	Pin	Signal Type	Pin Description
		level clock input i	syntax.
GND OALOG TO	Frequency m	anderd data rate. MHz ± 91%, and	Supply ground.
		O lator drive output this pin to XTAL 'L inputs used a	Drive Select-2 (active low). It enables the interface to this disk drive. This signal comes from the Operation Register. In Base mode, or Special mode, this output is #2 of the four decoded Unit Selects, as specified in the device command syntax.
MO1*, DS3*	is os 36 ator is y be driven	lator or External MHz Systal. Trita rates, and ma	Motor On enable for disk drive #1 (active low). This signal comes from the Operation Register. In Base mode, or Special mode, this output is #3 of the four decoded Unit Selects, as specified in the device command syntax.
MO2", DS4"	ed on 'he inne ogle "0" = 187	nsation Value. The compose stion us give "1" = 125 ns. It is used, PCV on is disabled.	Motor On enable for disk drive #2 (active low). This signal comes from the Operation Register. In Base mode, or Special mode, this output is #4 of the four decoded Unit Selects, as specified in the device command syntax.
(HCD) out LOH		(activeOow). High read (side) of the	Head Load (active low). When HDL* is low, causes the head to be loaded againt the media in the selected drive.
durrent to flow		ogic "1" = side 0 e (active low). "I ng on the diskets write head. Each falling edn tes a flux transife	Readuced Write Current / Revolutions Per Minute (active low). When low, causes a Reduced Write Current when bit density is increased toward the inner tracks, becoming active when tracks > 28 are accessed. This condition is valid for Base or Special mode, and is indicative of when write pre-compensation is necessary. In the AT/EISA mode, this signal will be active when CR0=1.
.noi c	= outward me	tive low), DIRC*c ir motor, Logic *i active low), STE	Disk Change (active low). This input senses status from the drive. Active low indicates that drive door is open or that the diskette has possibly changed since the last drive selection. It has internal pull-up.
*9W *erface to this alon Register.	novement of the 14 considers the information the Open	oh track to track i -1 (active low). I his signal comes	Write Protected (active low). This input senses status from disk drive, indicating active low when a diskette is Write Protected.
		le, or Special met it Selects, as spur	Track Zero (active low). This input senses status from disk

SYMBOL DESCRIPTION 11 and sish edit of the

Symbol	Pin	Signal Type	Pin Description
or mini Soppy	above double	nings mentioner rates.	drive, indicating active lowwhen the head is positioned over the outermost track, Track 00.
determine the	ince it could be	that in the non ine the Main St t of the interrupt ommand termin	begining of a track marked by an index hole.
VCC Dom AM	C65 44 the I	mai. If the ST3	

* 40 Pin package only

FUNCTIONAL DESCRIPTION AMO off (0 = 30AC)

ST37C65 includes data separation designed to address high performance error rate on floppy disk drives. It contains all the necessary Logic to achieve classical 2nd order, type 2, phase locked-loop performance. Write pre-compensation is included, in addition to the usual formatting, encoding/decoding, stepper motor control, and status sensing functions. All inputs are TTL compatible Schmitt Trigger line receivers, and outputs are high current, open drain, with 48 mA drivers which meet the ANSI specification.

The host interface supports an 8 or 12 MHz, 286 microprocessor bus without the use of wait states. The inputs are Schmitt Triggers. Output drive capability is 20 LS-TTL loads, allowing direct interconnection to bus structures without the use of buffers or transceivers. For PC, PC AT and EISA applications, qualification of interrupt request and DMA request is provided.

Traditionally, data rate selection, drive selection, and stepper motor control have been output ports of the host processor architecture. In the ST37C65, these functions are latched into registers addressed within the I/O mapping of the system. The ST37C65 has eight internal registers. The eight bit main status register contains status information about the

ST37C65 and may be accessed any time. Another four status registers under system control also give various status and error information. The. Control Register provides support logic that latches the two LSBs used to select the desired data rate that controls internal clock generation. The Operations Register replaces the standard latched port used in floppy subsystems. These registers are incorporated into the ST37C65.

CLOCK GENERATION what a nie M art ni TO bas 80

SCLK - Sampling Clock, WCLK- Write Clock, and MCLK - Master Clock, are included in the ST37C65. XTAL oscillator circuits provide the necessary signals for internal liming when using the 44 pin PLCC. If the 40 pin DIP is used, the TTL level clock inputs must be provided. There are two oscillator inputs to the ST37C65. The first at 32 MHz that handles all standard data rates (1Mb/sec, 500, 250, and 125 kb/sec or 16 MHz to handle 500, 250, and 125 Kb/sec.). The second oscillator is at 9.6 MHz to support the 300 kb/sec data rate used in PC AT designs.

Some AT compatibles use two-speed disk drives. If a two speed disk drive is used, the DRV input should be grounded along with the CLK2 input.

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ARCHITECTURE

The ST37C65 Floppy Disk Subsystem Controller is an LSI device that provides all the needed functionality between the host processor and the floppy disk drive. This "super-chip" integrates formatter/controller, data separation, write precompensation, data rate selection, clock generation, drive interface drivers and receivers.

HOST INTERFACE

The host interface is the Host Microprocessor Peripheral Bus. This bus is composed of eight control signals and eight data signals. In the Special or AT/EISA modes IRQ and DMA request are three-stated and qualified by DMA enable which is provided by the Operations Register. The data bus, DMA, and IRQ outputs are designed to handle 20 LS-TTL loading. Inputs are Schmitt Trigger receivers and can be hooked up to a bus or back plane without any additional buffering.

During the Command or Result phases, the Main Status Register must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data is read from or written into the Data Register, the CPU waits for 12µs before reading the Main Status Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of The command word may be written into the ST37C65. Many of the commands require multiple bytes. As a result, the Main Status Register must be read prior to each byte transfer to the ST37C65. During the Result phase, Bits D6 and D7 in the Main Status Register must both be 1's (D6=1 and D7=1) before reading each byte from the Data Register.

Note that this reading of the Main Status Register before each byte transfer to the ST37C65 is required only in the Command and Result phases, and not during the Execution phase. Note also that DB6 and DB7 in the MSR can be polled instead of waiting 12µs.

During the Execution phase, the Main Status Register need not be read. If the ST37C65 is in the non-DMA Mode, then the receipt of each data byte (ST37C65 is reading data from the FDD) is indicated by an interrupt signal on pin 16 (IRQ=1). The generation of a Read signal (RD*=0) clears the interrupt and sends the data

onto the data bus. If the processor cannot handle interrupts fast enough (every $13\mu s$ for the MFM mode and $27\mu s$ for the FM mode), then it may poll the Main Status Register and bit D7 (RQM) functions as the Interrupt signal. If a Write Command is in process then the WR* signal performs the reset to the Interrupt signal.

All timings mentioned above double for mini floppy data rates.

Note that in the non-DMA mode it is necessary to examine the Main Status Register to determine the cause of the interrupt since it could be a data interrupt or a command termination interrupt, either normal or abnormal. If the ST37C65 is in the DMA mode, no interrupt signals are generated during the Execution phase. The ST37C65 generates DMA's (DMA Requests) when each byte of data is available The DMA Controller responds to this request with both DACK*= 0 (DMA Acknowledge) and an RD*=0 (Read signal). When the DMA Acknowledge signal goes low (DACK*= 0), the DMA Request is cleared DMA= 0) If a Write Command has been issued, then a WR* signal will appear instead of RD*. After the Execution phase has been completed (Terminal Count has occurred) The EOT sector read/written, then an Interrupt will occur (IRQ=1) this signifies the begining of the result phase. When the first byte of data is read during the Result phase, the interrupt is automatically cleared (IRQ=0). Note that in PC AT usage, non-DMA Host transfers are not the normal procedure. If the user chooses to do so, the ST37C65 will successfully complete commands, but will at ways give abnormal termination error status since TC is qualified by an inactive DACK*. The RD* or WD* signals should be asserted while DACK* is true The CS* signal is used in conjunction with RD* and WR* as gating function during programmed I/O operations. CS* has no effect during DMA operations. It the non-DMA mode is chosen, the DACK signal should be pulled up to VCC.

Note that during the Result phase all bytes shown in the Command Table must be read.

The Read Data Command, for example has several bytes of data in the Result phase. All seven bytes must be read in order to successfully complete the Read Data command. The ST37C65 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during

the Result phase. The ST37C65 contains five Status Registers. The Main Status Register mentioned may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are available only during the Result phase and may be read only after completing a command. The particular command that has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the ST37C65 to form the command phase, and are read out of the ST37C65 in the result phase, must occur in the order shown in the Command table. The command code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result phases is allowed. After the last byte of data in the command phase is sent to the ST37C65, the Execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the result phase, the command is automatically ended and the ST37C65 is ready for a new command.

CONTROL REGISTER

The Control Register is a write only register that is used to set the data transfer rate and disable write precompensation. It provides support logic that latches

the two LSBs of the data bus upon receiving LDCR* and WR*. CS* should not be active when this happens. These bits are used to select the desired data rate, which in turn controls the internal clock generation. Clock switch over is internally "deglitched", allowing continuous operation after changing data rates. If the Control Register is not used, the data rate is governed by the supplied clock or crystal. The frequency must be 64 times the desired MFM data rate. This implies a maximum data rate of 250 kb/s for a frequency of 16 MHz or a maximum data rate of 500 kb/s for a frequency of 32 MHz, unless the Control Register is used. Switching of this clock must be "glitchess" or the device will need to be reset. Table 1 and Table 2 present the Control Register configuration for 16 MHz and 32 MHz frequencies, respectively.

ST37C65 optionally supports 150 kbits FM data transfer rate. The Control Register configuration is shown in Table 3. The 150 kb/s data rate can be selected by using a 9.6 MHz XTAL or TTL level clock input on pin 26 (44-pin PLCC) or pin 23 (40-pin DIP). Only two data transfer rates can be selected with this configuration 150 kb/s FM and 300 kb/s MFM.



TABLE 1. CONTROL REGISTER CONFIGURATION 16 MHz

STER STATUS	RPM (AT/EISA mode)	COMMENTS	DATA RATE	DRV	CR0	CR1
	tegister is an aight-bit, read	write MFM elitatet	500 k	X	0	0
	as the status information d	FM	250 k	X	0	0
	issed at any one. The ST3	MFM	250 k	0	1 8	0
ndes a write on	ly register, colled Master 8	MFM (9.6 MHz)	300 k	rengneri	r ng be	0
	which is used only to select p	MFM, RST Default	250 k	X	0	1
	rdown mode the XTAL oscil	FM, RST Default	125 k	X	0	1
	nd all linear of Julity are went of draws very lew current. No	FM Isma	125 k	X	SIBIQ MIT	1

TABLE 2. CONTROL REGISTER CONFIGURATION 32 MHz

CR1	CR0	DRV	DATA RATE	COMMENTS	RPM (AT/EISA mode)
0	0	X	stal and Market	MFM been	(esult phase and may be
0	0	X	500 k	oundres FM - 1840	a command. The part
0	site of	0	500 k	MFM	tenimeteb boluoess nec
0	yalei.	104×30	300 k	MFM (9.6 MHz)	gisters wilgo read.
8141 81	0	X	500 k	MFM, RST Default	1
1	0	X	250 k	FM, RST Default	on are sent to the \$1370
104 10	ple pist	X	250 k	FM	tuo eset sto bes team

TABLE 2. CONTROL REGISTER CONFIGURATION - OPTIONS

CR1	CR0	DRV	DATA RATE	COMMENTS	RPM (AT/EISA mode)
0	100	X	300 k	MFM	at byte of depois read out in
0	0	X	150 k	FM Page FM	immand is aytomalically end

In AT/EISA mode, write pre-compensation can be disabled by a logic high on bit-2 of the Control Register. (see table 4.)

TABLE 4. CONTROL REGISTER CONFIGURATION - AT/EISA MODE

віт	SIGNAL NAME AND FUNCTION	RESET	CLOCK QUALIFIER
0	Data rate	0	None
1	Data rate	0	None
2	No Write Pre-compensation	0	None
3-7	Reserved	None	None

MASTER STATUS REGISTER

The Master Status Register is an eight-bit, read/write register that contains the status information of the FDC. It can be accessed at any time. The ST37C65 provides a write only register, called Master Status Register 1 (MSR1) which is used only to select power down mode. In power down mode the XTAL oscillator, controller circuitry and all linear circuitry are turned off so that the controller draws very low current. Normal operation is restored by asserting reset to the ST37C65 (see Master Status Register 1).

Only the Master Status Register may be read and used to facilitate the transfer of data between the processor and ST37C65. The DIO and RQM bits in the Master Status Register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last RD* or WR* during a Command or Result phase and the setting of DIO and RQM is 12µs if 500 kb/s MFM data rate is selected. (If 250 kb/s MFM is selected, the delay is 24µs. If 1 Mb/s is selected, the delay is 6µs.) For this reason, everytime the Master Status Register is read, the CPU should wait 12µs. The maximum time from

the trailing edge of the last RD* in the result phase to when DB4 (FDC busy) goes low is $12\mu s$.

MASTER STATUS REGISTER 1

(MSR1 - Write Only)

The ST37C65 will enter power down mode, when bit of MSR1 is set to logical "1" and the following conditions are met:

1. The RST pin to the FDC is inactive.

2.Bit 2 in the Operations Register is "SRST= 1".

3. The ST37C65 is a waiting a command from the host

The ST37C65 can also be programmed with external logic to automatically enter power down mode a few msec. after the beginning of idle mode.

Normal operation is restored when the RST pin to the FDC is active and the FDC is reset. This in turn resets bit of MSR1 register to logic 0.

TABLE 5. AT/EISA MODE. MASTER STATUS REGISTER 1 CONFIGURATION

BIT	SIGNAL NAME AND FUNCTION	RESET	CLOCK QUALIFIER
0	Power down mode (PDM)	0	None
1-7	Reserved	None	None

TABLE 6. MASTER STATUS REGISTER BITS

BIT	NAME	SYMBOL	DESCRIPTION
D0	FDD 0 busy	of DOB and	FDD number is 0 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE command.
D1 = 9	FDD 1 busy	D1B	FDD number is 1 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE command.
D2	FDD 2 busy	D2B	FDD number is 2 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE command.
D3	FDD 3 busy	D3B	FDD number is 3 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE command.
D4	FDC busy	CB CB	A READ or WRITE command is in progress. FDC will not accept any other command.
D5	Execution mode	EXM	This bit is set only during execution phase in non-DMA mode. When D5 goes low Execution phase has ended and Results Phase has started. It operates only during non-DMA mode of operation.

BIT	NAME	SYMBOL	DESCRIPTION
D6 wet a s	Data input	TCC OID also automatically iter tine beginn operation is ne	Indicates direction of data transfer between FDC and Data Register. If DIO = 1, then transfer is from Data Register to the processor. If DIO = 0, then transfer is from the processor to Data Register.
D7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the handshaking function of "ready" and "direction" to the processor.

TABLE 7. STATUS REGISTER 0 BITS

NAME	SYMBOL	DESCRIPTION
Unit select 0	US0	This flag is used to indicate a Drive Unit Number at interrupt
Unit select 1	US1	This flag is used to indicate a Drive Unit Number at interrupt
Head select	HS	This flag is used to indicate the state of the head at interrupt
Not ready	NR	Since drive Ready is always presumed true, this will always be a logic "0" (low).
and the same of the same of		
Interrupt code	A stand Control	See D7. ggg 850 yand \$ ggg 950
Interrupt code death of the black of the bla	OI in the Seek N ept READ or N	D7 = 1 and D6 = 0, invalid command issue. Command which was issued was never started.D7 = 0 and D6 = 0, normal termination of command was completed and properly executed. D7 = 0 and D6 = 1, abnormal termination of com-
	Unit select 0 Unit select 1 Head select Not ready Equipment check Seek end Interrupt code Interrupt code	Unit select 0 US0 Unit select 1 US1 Head select HS Not ready NR Equipment check EC Seek end SE

TABLE 8. STATUS REGISTER 1 BITS

BIT	NAME	SYMBOL	DESCRIPTION
D0	Missing address mark	terk AM ata DC cannot ress Mark, t	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. At the same time the MD (Missing Address Mark in data field) of Status Register 2 is set.
edthe	that stored in the IDR ar	nont trensfill	en the medium is
	Not writeable par		During execution of Write Data, Write Deleted Data of Format a Track commands, if the FDC detectes a WP*signation from the FDD, then this flag is set.
D2 to no	No data	ND IAS SCALE IN THE REAL OF THE PAIR DESTRUCTION AND DESTRUCTI	During execution of Read Data, Write Deleted Data, or Scar command, if the FDC cannot find the sector specified in the IDR (Internal Data Register), this flag is set. During execution of the Read ID command, if the FDC cannot read the ID field without an error, then this flag is set. During execution of the Read a Track command, if the starting sector cannot be found, then this flag is set.
D3	Not used		This bit is always set to "0".
D4	Overrun	OR	If the FDC is set not serviced by the host system during data transfers within a certain time interval, this flag is set.
D5	Dollar Data error of the	of the Read a se30 w s flag is set	When the FDC detects a CRC (Cyclic Redundancy Check error in either the ID field or the data field, this flag is set.
D6	Not used	."0" of fee	This bit is always set to "0".
D7	End od cylinder	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.



TABLE 9. STATUS REGISTER 2 BITS

2.40	DESCRIPTION	SYMBOL	NAME	BIT
ind a Data Address Mark of		nole twice, the b Data Addres		FDC ta Ad-
that stored in the IDR and th	This bit is related to the ND bit on the medium is different from contents of C is FF, then this f	data (IBC) etab	Bad cylinder	D1 -
	During execution of the SCAN find a sector on the cylinder who this flag is set.	en thiNZag is of Read Data,		D2
	During execution of the SCAN "equal" is satisfied, this flag is	a RegH2r), thi mmand, if the	Scan equal	D3 luo bleft C
	This bit is related to the ND bit, on the medium is different from is set.	the Wommo		
Not used -	This bit is always		of Vigitable and suited	-
numeyO			Data error the host system durin nterval, this flag is set	
	During execution of the Read D FDC encounters a sector whi	MO letects a CRC	Control mark	D6 (Non1)
	Address Mark, this flag is set.	int re bleit Of a	data field, this flag is	set.
	This bit is always set to "0".	"0" of les	Not used	D7

TABLE & STATUS REGISTER 1 BITS

TABLE 10. STATUS REGISTER 3 BITS

BIT	NAME	SYMBOL	DESCRIPTION
D0	Unit select 2	US0	This bit is used to indicate the status of the Unit Select 0 signa to the FDD.
D1 , then	Unit select 1	US1 levilve active.	This bit is used to indicate the status of the Unit Select 1 signa to the FDD.
D2	Head select	ede. SH to become act	This bit is used to indicate the status of the Side Select signate to the FDD.
D3	Write protected	WP*	This bit is used by the ST37C65 to indicate the status of the Write Protected (WP*) signal from FDD.
D4	Track 0	то	This bit is used to indicated the status of the Track 0 signal from the FDD.
	\T/IEISA.mode.	active only in	
D5	Ready	YS active only in	This bit will always be a logic "1". Drive is presumed to be ready.
D6	Write protected	WP*	This bit is used to indicate the status of the Write Protected (WP*) signal from FDD.
mode	elect between Special	nay be used to	OR7 (MSEL) Mode Select. During a soft reset condition;
D7	Not used		This bit is always set to "0".

DATA REGISTER

The eight-bit Data Register stores data, commands, parameters, and FDD status information. Data bytes are read out A0, or written into, the Data Register in order to program or obtain the results after a particular

command.The relationship between the Master Status Register and the Data Register and the signals RD*, WR*, and A0 are shown in Table 11.

Table 11. MASTER STATUS AND DATA REGISTER

A0	RD*	WR*	FUNCTION	
B 00	000	mil n ip	Read Main Status Register	il e
isiosq2	neins e	0	any software driver lapallle reset, 8	
0 0X	1000	0	ase mode, the Opelagelli Registe	
en1dea	000	0	ster X 0 X X), setti lagallide Selec	36
evijas	00	R2pni	Read from Data Register	
"RPC.	ddrhss.	190	Write into Data Register	
	de. The	m Islos	ier. and places the device in Sp	

OPERATIONS REGISTER

The Operations Register provides support logic that latches the data bus upon receiving LDOR* and WR*. CS* should not be active when this happens. The

Operations Register replaces the typical latched port found in floppy subsystems used to control disk drive spindle motors and to selected the desired disk drive. Table 12 represents the Operations Register.

TABLE 12. OPERATIONS REGISTER

OR0	DSEL	Drive Select, if low and MOEN1 = 1, then DS1* is active. If high and MOEN2 = 1, then DS2* is active, but only in the AT/IEISA mode.
OR1	(X)	This must be a logic 0 for DS1* and DS2* to become active.
OR2	SRST*	Soft reset, active low. a beau at the ain?
OR3	DMAEN	DMA enable, active in Special and AT/EISA modes. Qualifies DMA and IRQ output and DACK* input.
OR4	MOEN1	Motor On enable, inverted output M01* is active only in AT/IEISA mode.
OR5	MOEN2	Motor On enable, inverted output M02* Is active only in AT/EISA mode.
OR6	9 (X)/ e	Has no defined function. A spare.
OR7	(MSEL)	Mode Select. During a soft reset condition, may be used to select between Special mode (1) and AT/IEISA mode (0).

BASE, SPECIAL, AND AT/EISA MODES

Base, Special, PC AT and EISA modes allow subtle differences which the user may find desirable. The Control Register may be used in any mode without altering functionality.

Base Mode

After a hardware reset, RST active, the ST37C65 will be held in soft reset, SRST* active, with the normally driven signals, DMA request and IRQ request outputs three-stated. Base mode may be initiated at this time by a chip access by the host. Although this may be any read or write, it is strongly recommended that the Base mode user's first chip access be a read of the Master Status Register. Once Base mode is entered, the soft reset is released, and IRQ and DMA are driven. Base mode prohibits the use of the Operations Register,

hence there can be no qualifying DMAEN and no soft resets. The Drive Select outputs, DS1* to DS4*, offer a 1 of 4 decoding of the Unit Select bits resident in the command structure. Pin RWC* represents Reduce Write Current and is indicative of when write precompensation is necessary.

Special Mode

Special mode allows use of the Operations Register for the DMAEN signal as a qualifier and to do a software driven device reset, SRST*. To enter Special mode, the Operations Register is loaded with (1 X 0 0 X 0 X X), setting mode Select to a logic 1 disabling MOEN1 and MOEN2 and causing SRST* to be active. Then a read of the Control Register address, LDCR* and places the device in Special mode. The DS1*

through DS4* is again offered in this mode, as is RWC*.

When PCVAL pin (24)=1, all data will seboth AZIS/TA

For AT/EISA compatibility, users write to the Operations Register, LDOR* and WR*; this action, performed after a hardware reset, or in the Base mode. initiates AT/EISA mode. AT/EISA mode can also be entered from Special mode by loading the Operations Register with (0 X 0 0 X 0 X X), setting Mode Select to a logic 0, disabling MOEN1 and MOEN2, and causing SRST* to be active. Then a read of the Control Register address sets the device into AT/EISA mode. The DS* outputs are replaced with the DSEL and MOEN signals buffered from the Operations Register. DMAEN and SRST* are supported and compatible with the current BIOS. RWC* pin function is now RPM* so that users with two-speed drives may reduce spindle speed from a nominal 360 revolutions per minute to 300 revolutions per minute when active low. It can also be used to reduce write current when a slower data rate is selected for a given drive. the ST37C65, They are: Sampling Clock (SCLK),

SCLK drives the WD92C32 Data SeparA SAUDIA

DS4*

DRIVE SELECT POLLING TIMING (beau at) LIOW

se scheme. One mi*tag Data Rate. DS2* In power down mode the XTAL oscillator and the clok circultry are turned off DS3*

POLLING ROUTINE

After any reset the ST37C65, (a hard RST or soft SRST*), will automatically go into a Polling routine. In between commands (and between step pulses in the SEEK Command), the ST37C65 polls all four FDDs looking for a change in the Ready line from any of the drives. Since the drive is always presumed Ready, an interrupt will only be generated following a reset. This occurs because a reset forces Not Ready status, which then promptly becomes Ready. Note that in Special, AT/EISA modes, if DMAEN is not valid 1ms after reset goes inactive, then IRQ may be already set and pending when finally enabled onto the bus. The polling of the Ready line by the ST37C65 occurs continuously between Each drive is polled every 1.024ms, except during the READ/WRITE commands. For mini- floppies, the polling rate is 2.048ms. The drive polling sequence is 1-2-4-3. Note that in the AT/EISA mode, the user will not see the polling at the Drive Select signals. Figure 4 illustrates the Drive Select Polling Timing. and Issai babnaka

The Data Separator is a WD92C32 Digital Phase Lock

should be applied. The EARLY and LATE signals are Ancoded VVRITE signal is synchronized to the 16 MHz or 32 MHz through a shift register. Signals EARLY, NOM, and register betyre a multiplexed gates the chosen bit to the output. The output data bulks width has a 25% duty

DEVICE RESETS

The ST37C65 supports both hardware reset (RST pin 19) and a software reset (SRST*) through use of the Operations Register. The RST pin will cause a device reset for the active duration. RST causes a default to Base mode, and selects 250kb MFM (or 125kb FM code dependent) as the data rate (16 MHz input clock) The default data rate for a 32 MHz input clock is 500kb MFM. SRST* will reset the micro controller as did the RST, but will not affect the current data rate selection or the mode RST, when active, will disable the current driver outputs to the disk drive. RST and SRST* will not affect the values set for the internal timers HUT, HTL, and SRT.

If the XTAL oscillators are used, instead of the TTL driven clock inputs, the hardware RST active time requirement will be extended. The oscillator circuit is designed so that RST will bootstrap the circuit into guaranteed oscillation in a fixed amount of time. The extended reset time allows the growth of the oscillation to produce stable internal clock timing.

DATA SEPARATOR

The Data Separator is a WD92C32 Digital Phase Lock Loop Floppy Disk Data Separator (DPLL). It was designed to address high performance error rates on floppy disk drives, and to provide superior performance in terms of available bit jitter tolerance. It contains the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance. Figure 1 illustrates the WD92C32 used as the Data Separator in the ST37C65 system. The bit jitter tolerance for the data separator is 60%, which guarantees an error rate of <10E-9.

WRITE PRE-COMPENSATION

The ST37C65 maintains the standard first level algorithm to determine when write pre compensation should be applied. The EARLY and LATE signals are used internally to select the appropriate delay in the write data pulse stream. The encoded WRITE DATA signal is synchronized to the 16 MHz or 32 MHz clock if this is the frequency on CLK1 pin (23), and clocked through a shift register. Signals EARLY, NOM, and LATE determine the amount of delay through the shift register before a multiplexed gates the chosen bit to the output. The output data pulse width has a 25% duty

cycle, i.e., one fourth of the bit cell period, and equal to one half the WCLK period.

When PCVAL pin (24)=1, all data will be pre-compensated by ±125ns, regardless of track number and data rate. However, this is only for MFM encoding. There is no write pre-compensation for FM. If PCVAL = 0, and if a track inside number 28 is accessed, then ±187ns pre-compensation will be generated. For frequencies other then 16MHz or 32MHz on the CLK1 pin, the precompensation values will be two and three clock cycles respectively. When the non-standard 300 kb/ s data rate using CLK2 is chosen, the MFM precompensation will always be two clock cycles For 9.6 MHz, this is ±208ns. In this case, the PCVAL function is disabled. Write pre-compensation can be disabled by bit-2 of the Control Register for the AT/EISA. The PCVAL input to ST37C65 is ignored if there is no write pre-compensation.

CLOCK GENERATION

This logical block provides all the clocks needed by the ST37C65. They are: Sampling Clock (SCLK), Write Clock (WCLK), and the Master Clock (MCLK). SCLK drives the WD92C32 Data Separator used during data recovery. This clock's frequency is always 32 times the selected data rate.

WCLK is used by the encoder logic to place MFM or FM on the serial WD-stream to the disk. WCLK always has a frequency two times the selected data rate.

MCLK is used by microsequencer. MCLK and MCLK* clock all latches in a two-phase scheme. One micro-instruction cycle is four MCLK cycles. MCLK has a frequency equal to eight times the selected MFM data rate or 16 times the FM data rate. Table 13 presents the Clock Data Rate.

In power down mode the XTAL oscillator and the clok circuitry are turned off.

TABLE 13. CLOCK DATA RATE

DATA RATE	CODE	SCLK	MCLK	WCLK	94			
43.00-4-	1,5000	MSMMDO						С ИАММОЗ
1Mb/s	MFM	32.0 MHz	8.0 MHz	2.0 MHz				
500 kb/s	MFM	16.0 MHz	4.0 MHz	1.0 MHz				
500 kb/s	FM	16.0 MHz	8.0 MHz	1.0 MHz				
250 kb/s	FM	8.0 MHz	4.0 MHz	500 kHz				
250 kb/s	MFM	8.0 MHz	2.0 MHz	500 kHz				
125 kb/s	FM	4.0 MHz	2.0 MHz	250 kHz				
300 kb/s	MFM	9.6 MHz	2.4 MHz	600 kHz				

COMMAND PARAMETERS

The ST37C65 is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor. The results after execution of the command may also be a multibyte transfer back to the processor. The commands consist of three phases: Command phase, Execution phase, and the Result phase.

- Command phase
 The Floppy Disk Controller (FDC) receives all information required to perform a particular operation from the processor.
- Execution phase
 The FDC performs the operation it was instructed to do.
- Result phase
 After completion of the operation, status and other housekeeping information are made available to the processor.

Table 14 lists the 15 ST37C65 commands.

TABLE 14. ST37C65 COMMANDS

- Read Data
- Read Deleted Data
- Write Data
- Write Deleted Data
- Read a Track
- Read ID
- Format a Track
- Scan Equal
- Scan Low or Equal
- Scan High or Equal
- Recalibrate
- · Sense Interrupt Status
- Specify
- Sense Drive Status
- Seek

4

TABLE 15, READ DATA

PHASE	R/W	D7	D6	D5	D4	D3 D	2 D1	D0	DESCRIPTION
COMMAND	W W W	MT X	MF X	SK X	0 X	1 0 0 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1		0 1 USO 4 0.8 4 0.8 4 0.8 4 0.8 4 0.8	Sector ID informatiom prior to command execution. The four bytes are compared against header on floppy disk.
	W W W	,				N EOT GPL DTL			
EXECUTION	BGHAN	MOD	C65	TETE	14.8	TABLE			Data transfer between FDD and main system.
RESULTS	R	Brad .			d Dat	CTO		ig 15 di im a yd	Status information after com-
	R R R	0.1				ST1 ST2 C	execu ransfe of three	s after tlibyte t consist o shase, a	Sector ID information after com-
	R R R			TO W		R N		ieoen (esult phase. Command phase The Floppy Disk Controller (FDC

Specify
 Sense Drive Status

· Sense Interrupt Status

er completion of the operation, status and other isekeeping information are made available to processor.

TABLE 16. READ DELETED DATA

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	DESCRIPTION
COMMAND	W	МТ	MF	SK	0	0	1	1	0	0	Command code.
	W	X	X	X	X		X	HS	US1	US0	XXXW
			notos			C					Sector ID informatiom prior to
											command execution. The four
											bytes are compared against
	oppy di	in no.									header on floppy disk.
	W					Н					W
	W					R					W
	W			10 1		N					W
	W					EOT					W
	W					GPL					W
	W					DTL					W
EXECUTION	ewied 1	ansie									Data transfer between FDD and
		netey									main system.
RESULTS	R	olni				ST0					Status information after com-
	noit	JOSKE									mand execution.
	R					ST1					9
	R					ST2					9
	1,	ni QI				C					Sector ID information after com-
	tion.	изехв		m							mand execution.
	R					H					Я
	R					R					8
	R					N					8



TABLE 17. WRITE DATA

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	DESCRIPTION
COMMAND	Woo	МТ	MF	0	0	0	0	1	0	1	Command code.
	W	X	X	X	X		X	HS	US1	US0	X X X W
						C					Sector ID informatiom prior to
											command execution. The four
	1.										bytes are compared against
	oppy d	II no									header on floppy disk.
	W					H			Н		W
	W					R					W
	W					EOT					W
	W					GPL					W
	W	No.				DTL					W
	00					DIL					VV
EXECUTION	wied w	ansfi Jaten									Data transfer between FDD and main system.
RESULTS		ofni				ST0					Status information after com-
	R					ST1					Я
	R					ST2					g l
	SR o	ni Gi				C					Sector ID information after com-
	.noBi	eo exe									mand execution.
	R					Н					Я
	R					R					Я
	R	1				N					Я

TABLE 18. WRITE DELETED DATA

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	DESCRIPTION
COMMAND	Woo	MT	MF	0	0	Ť	1	0	0	1	Command code. QUAMMOO
	W	X	X	X	X		X	HS	US1	US0	XXXW
	W	I OI	ector			C			0		Sector ID informatiom prior to
											command execution. The four
	egmes	916									bytes are compared against
	oppy dis	it no t		rd.							header on floppy disk.
	W					Н					W
	W					R					w C
	W					N			N		W
	W	1 11				EOT			TO3		W
	W	12			(GPL					W
	W				- 1	DTL					W
EXECUTION	awtari ne	atengr		a l							Data transfer between FDD and
											main system.
RESULTS	R	1				ST0					Status information after com-
	noitem	olni									mand execution.
	Rom	ровхе				ST1					
	R					ST2			STI		9
	R					C					Sector ID information after com-
	formatic	ni Ol-									mand execution.
	R	рэхв				Н					
	R					R					Я
	R	1				N					9

TABLE 19. READ TRACK

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	DESCRIPTION
COMMAND	W	МТ	MF	-	0	0	0	0	1	0	Command code.
	W	X	X	X	X		X	HS	US1	US0	XXXXIW
						C					Sector ID informatiom prior to
											command execution. The four
		C - S - S - S - S - S - S - S - S - S -									bytes are compared against
	10230-4-0	n no									header on floppy disk.
	W	1 1 3 4				Н					W
	W	er si				R					W
	W	096				N					W W
	W					EOT					W
	W					GPL					VV
	W	1-13				DTL					W I W I
EXECUTION	wied n	ansig									Data transfer between FDD and
	a	netay									main system. FDD reads all data fiels from index hole to EOT.
	onation	info									RESULTS R
RESULTS	R	Dexe				ST0					Status information after com-
	Mina.										mand execution.
	R					ST1					8
	R	ni Ol				ST2					A Property
	R	DON				C					Sector ID information after com-
	1	143									mand execution.
	R					Н					8
	R	i lite				R					7
	R					N					

PHASE	R/W	D7 D6 D5	D4 D3	3 D2 D1 D0	DESCRIPTION
COMMAND of noise most	W	0 MF 0 X X X	X USI X	0 1 0 HS US1 US0	Command code.
		command e		H SI M	The first corrected ID information on the cylinder is stored in Data Register.
RESULTS	R		ST0		Status information after com- mand execution.
	R R		ST1 ST2		TW
		Data compa and main sy	С		Sector ID information read during Execution Phase from floppy disk.
		Status info	H		RESULTS R
	R		N	ST1	R R

TABLE 21. FORMAT A TRACK

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	DESCRIPTION
COMMAND	W	0 X	MF X	0 X	0 X		1 X	1 HS	0 US1	1 US0	Command code.
	W W W					N SC GPL D					Bytes/Sector. Sectors/Track. Gap 3. Filler Byte.
EXECUTION											Floppy Disk Controller (FDC) formats an entire track.
RESULTS	R	183				ST0					Status information after com- mand execution.
	R					ST1					mand excedition.
	R	J. III				ST2					
	R					С					In this case, the ID information has no meaning.
	R					Н					nas no meaning.
	R					R				100	
	R	1				N					

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	D	ESCI	RIPT	ION	
COMMAND	W	MT	MF X	SK X	1 X	180	0 X	0 HS	0 US1	1 US0	С	omm	and o	code.	COMMAND
	W	137				C	413	1 2 3			S	ector	ID i	nforma	tiom prior to
											C	omma	and e	xecutio	EXECUTION.n
	W					H R									
	W					N									
	W	into				EOT									
	W	uoaxs				GPL									
	W	100				STP									
EXECUTION	termo	hmi CU									D	ata co	ompa	red bety	ween the FDD
	pesn ^c										a	nd ma	ain sy	stem.	
DE01 T0	_														
RESULTS	R					ST0						tatus and e			n after com-
	R					ST1			g U		1	iana (CACCI	Ation.	
	R					ST2									
	R					С								formati ution.	on after com-
	R					Н					"				ABLE 21, FOR
	R					R									
	1810	11 712									aa.				
	,ebo	and c									0				
					081	tau	SH.	X		X	X	X	X	W	
														W	
														W	
		lyte. Disk												W	
		yte. Disk n enti												W	
		lyte. Disk n n enti												W	
		yte. Disk n enti												W W	
		lyte. Disk n n enti												W W A A	
		lyte. Disk n n enti krios execu												W W	
		lyte. Disk n n enti krios execu												W R R R R R R R R	
		lyte Disk in entit kirlor execut												WW R RR	

TABLE 23. SCAN LOW OR EQUAL

W X X X X X HS US1 US0 W C Sector ID informatiom prior to command execution. W H R N SECT GPL W DTL EXECUTION Data compared between FDE and main system.	PHASE	R/W	D7 D6	D5	D4 D3	D2 D1 D	0 DESCRIPTION
W H R N SECUTION EXECUTION RESULTS R ST0 R ST1 R ST2 R C Sector ID informatiom prior to command execution. Sector ID information prior to command execution. Sector ID information prior to command execution. Status information after command execution. Status information after command execution. Sector ID information after command execution.	COMMAND						
Command execution. W W R N N EOT GPL W DTL EXECUTION RESULTS R ST0 Status information after command execution. R ST1 R ST2 R C Sector ID information after command execution. R R R R R		-	XX	X	X	HS US1 US	
EXECUTION RESULTS R ST0 Status information after command execution. R R R ST1 R R ST2 R R R R R R R R R R R R R R R R		W			С		Sector ID informatiom prior to command execution.
EXECUTION RESULTS R ST0 Status information after command execution. R R R R R R R R R R R R R		W			Н		W
EXECUTION RESULTS R ST0 Status information after command execution. R R R R R R R R R R R R R		W			R		W
EXECUTION RESULTS R ST0 Status information after command execution. R R R C Sector ID information after command execution. R R R R R R R R R		W			N		W
EXECUTION RESULTS R ST0 Status information after command execution. R R ST1 R C Sector ID information after command execution. R R R R R R R		W			EOT		W
EXECUTION RESULTS R ST0 Status information after command execution. R R ST1 R C Sector ID information after command execution. R R R R R R		W			GPL	390	W
RESULTS R ST0 Status information after command execution. R R ST1 R C Sector ID information after command execution. R R R R R R		W			DTL		W
RESULTS R ST0 Status information after command execution. R R ST2 R C Sector ID information after command execution. R R R R R	EXECUTION	d ber	ia compa				Data compared between FDD
mand execution. R ST1 R ST2 C Sector ID information after command execution. R H R R		.mex	iya nisin t				and main system.
R ST1 R ST2 R C Sector ID information after command execution. R R R	RESULTS	R	totni auto		ST0		Status information after com-
R ST2 C Sector ID information after command execution.			nd execu				mand execution.
R C Sector ID information after command execution. R R R							
R H R R		1					A PERSONAL PROPERTY OF THE PRO
R R					С		
		R			Н		S S S S S S S S S S S S S S S S S S S
R N					R		4 9
		R			N		A Part of the second of the se



TABLE 24. SCAN HIGH OR EQUAL

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	DESCRIPTION
COMMAND	W	MT	MF	sk	1	0	10	1	0	1	Command code.
	W	X	X	X	X		X	HS	US1	US0	XXXX
	Work					С					Sector ID informatiom prior to command execution.
	W					Н					W
	W					R					W
	W					N					W
	W					EOT					W
	W					GPL					W
	W					STP			JTC		W
EXECUTION		ompa in syd									Data compared between FDD
	101011	-4c H									and main system.
RESULTS		iafer xecu				ST0					Status information after com- mand execution.
	R					ST1					9 19 1
	R					ST2					9
-тор тала по	R	Ini Gi				C					Sector ID information after com-
	ion.	UOSX									mand execution.
	R					Н					R I I
	R					R					R
	R					N					R

TABLE 25. RECALIBRATE

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	0 X	0 X	0 X	0 X	0 X	1 0	1 US1	1 US0	Command code.
EXECUTION										Head retracted to Track zero.

TABLE 26. SENSE INTERRUPT STATUS

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	DESCRIPTION
COMMAND	W					nella				0 US0	Command code. 0A
RESULTS	R	i) net				ST0 PCN					Status information about the FDC at the end of seek operation.

TABLE 27. SPECIFY

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION	
COMMAND	W	0	0	0	0	0	0	1	1	Command code.	
	W	SRT	SRT	SRT	SRT	HUT	HUT	HUT	HUT		103
	W	HLT	ND								
									09 -11		

TABLE 28. SENSE DRIVE STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2 D1 D0	DESCRIPTION
COMMAND	W	0	0	0	0	0	1 0 0	Command code.
	W	77000	X				HS US1 US0	
RESULTS	R							Status information about FDC.

TABLE 29. SEEK ATM dolder hit decision as show MT work TM III

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1 D0	DESCRIPTION
COMMAND	W	all and				e2 101 1 m	1	9-1	Command code.
	W		X					US1 US0	
	W	hy ae			-	ICN			N Number
EXECUTION	mw StE	EMI,							Head is positioned over proper
	barisa	3.00							cylinder on the diskette.

TABLE 30. COMMAND SYMBOL DESCRIPTIONS SUTATE TRUPPER SENSE 38. SUBAT

SYMBOL	NAME	DESCRIPTION
A0	Address line 0	A0 controls selection of Main Status Register (A0=0) or Data Register (A0=1).
	oda Cylinder Numbera	C stands for the current/selected cylinder (track) number 0 through 255 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector
D7 - D0	Data Bus	8-bits Data Bus, where D7 stands for a most significant bit, and D0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the Data length which users are going to read out or write into the sector.
EOT	End of Track	EOT stands for the final sector number on a cylinder. During Read or Write operations, FDC will stop data transfer a sector numbe equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During the FORMAT Command it determines the size of Gap 3.
Н	Head Address	H stands for head number 0 or 1, as specified in the ID field.
HLT	Head Load Time	HLT stands for the Head Load Time in FDD (2 to 254 ms in 2 ms increments).
HS .009 to	Head Select	HS stands for a selected head number 0 or 1 and controls the polarity of pin 25 (in 40 pin DIP) or pin 28 (in 44 pin PLCC).
HUT	Head Unload Time	HUT stands for the HEAD UNLOAD TIME after a Read or Write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM	If MF is low, FM mode is selected. If it is high, MFM mode is selected
MT	MultiTrack	If MT is high, a MUTITRACK operation is performed. If MT=1 after
	Command code.	finishing Read/Write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
N	Number	N stands for the NUMBER of data bytes written in a sector.
NCN	New Cylinder Number	NCN stands for a NEW CYLINDER NUMBER which is going to be reached as a result of the Seek operation. Desired position of head
ND	Non-DMA Mode	ND stands for operation in the NON-DMA MODE.

TABLE 30. COMMAND SYMBOL DESCRIPTIONS

SYMBOL	NAME	DESCRIPTION
PCN	Present Cylinder	PCN stands for the cylinder number at the completion of the SENSE INTERRUPT STATUS Command. Position of head ar present time.
R	Record	R stands for the sector number which will be read or written.
R/W	Read/Write	R/W stands for either READ or WRITE signal.
sc	Sector	SC indicates the number of sectores per cylinder.
SK	Skip	SK stands for SKIP Deleted Data Address Mark.
SRT	Step Rate Time	SRT stabds for the Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). Stepping Rate applies to all drives. In 2's complemen format, F (hex)=1 ms, E (hex)=2 ms, etc.
ST0-3	Status 0-3	ST0-3 stands for one of four registers which store the STATUS information after a command has been executed. This information is available during the result phase after command execution These registers should not be confused with the Main Status Register (selected by A0=0). ST0-3 may be read only after a command has been executed and contains information relevant to that particular command.
STP	15 at side 1 15 at side 1	During a SCAN operation, If STP=1, the data in contiguous sectors is compared byte by byte with data sent from the processor (o DMA); if STP=2, then alternate sectore are read and compared.
US0-1	Unit Select 0-1	US stands for a selected drive; binary encoded, 1 of 4.

COMMAND DESCRIPTIONS

Read Data

A set of nine byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time Idefined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read of the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the dala bus. After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next seclor is read and output on the data bus. This continuous read function is called a "Multi- sector Read Operation" The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time thal the DACK* for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data command. The amount of data which can be handled with a single command to the FDC depends upon MT (multItrack), MF (MFM/FM), and N (number of bytes sector). Table 31 lists the Transfer Capacity.

TABLE 31. TRANSFER CAPACITY

Multi- Track MT	MFM/ FM MF	Bytes/ Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskettes		
0	0 00 1 01		(128) (26) = 3328 (256) (26) = 6656	26 at side 0 or 26 at side 1		
	0	00 01	(128) (52) = 6656 (256) (52) = 13312	26 at side 1 26 at side 1		
0	0	01 02	(256) (15) = 3840 (512) (15) = 7680	15 at side 0 or 15 at side 1		
1 1 2 2 2	0	01 02	(256) (30) = 7680 (512) (30) = 15360	15 at side 1 15 at side 1		
0	0	02 03	(512) (8) = 4096 (1024) (8) = 8192	8 at side 0 8 at side 1		
1	0	02 03	(512) (16) = 8192 (1024) (16) = 16384	8 at side 1 8 at side 1		

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette. When N=0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond

DTL in the sector is not sent to the Data Bus. The FDC reads (internaily) the complete sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read operation. When N is non-zero, then DTL has no meaning and should be set to FF hexidecimal.

At the completion of the Read Dala command, the head is not unloaded until after Head Unload Time

Interval (specified in the Specity command) has elapsed. If the processor issues another command before the head unloads, then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another If the FDC detects the Index Hole twice without finding the right sector, (indicated in 'R'), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 Io 1 (high). If a CRC error occurs in the Data Field, the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data command. (Status Register 0 also has bits 6 and set to 0 and 1) respectively.

If Ihe FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit OS in the first Command Word) is not set (SK=0) then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data command after reading all the data in the sector. If SK=1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK=1.

During disk data transfers between the FDC and the processor via the data bus, the FDC must be serviced by the processor every $27\mu s$ in the FM mode, and every $19\mu s$ in the MFM mode or the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high), and terminates the Read Data command. If the processor terminates a read (or write) operation in the FDC, then the ID information in the Result phase is dependent upon the state of the MT bit and EOT byte. Table 32 shows the values for C, H, A, and N, when the processor terminates the command.

TABLE 32. C, H, R, AND N VALUES 101 bns/filmob

		Final Sector Transferred	ID Information at Result Phase						
MT	HD	to Processor	С	Н	R	N			
0	0	Less than EOT	NC	NC	R+1	NC			
0	0	Equal to EOT	C+1	NC	R=1	NC			
0	_1	Less that EOT	NC	NC	R+1	NC			
0	1	Equal to EOT	C+1	NC	R=1	NC			
110	0	Less than EOT	NC	NC	R+1	∍NC			
1.9	0	Equal to EOT	NC	LSB	R=1	NC			
1	9	Less than EOT	NC	NC	R+1	NC			
1	21181	Equal to EOT	C+1	LSB	R=1	NC			

Note: NC (No Change): The same value as the one at the begininning of command execution.

Write Datas

A set of nine bytes is required to set the FDC into the Wide Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD.

After writing data into the current sector, the sector number stored in 'R' is incremented by one, and the next data field is written into. The FDC continues this 'Multisector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent complete the data field. If the Terminal Counl signal is received while a data field is being written, then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes in one of the ID fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high) and terminates the Wrile Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write command operates in much the same manner as the Read command. The following items are the same, and one should refer to the Read Data

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command for details

- Transfer capacity
- . EN (End of Cylinder) flag
- ND (No Data) flag
- Head Unload Time interval
- ID Information when the processor terminates command
- Definition of DTL when N = 0 and when N= 0

In the Write Data mode, data transfers between the processor and FDC via the data bus, must occur every $27\mu s$ in the FM mode and every $13\mu s$ in the MFM mode. If the time interval between data transfers is longer than this, then the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high) and terminates the Write Data command (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

Write Deleted Data

This command is the same as the Write Data command except a Deleted Data Address mark Is written at the beginning of the data field instead of the normal Data address mark.

Read Deteted Data.

This command is the same as the Read Data command except that when the FDC detects a Data Address mark at the beginning of a data field (and SK=0) it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK=1, then the FDC skips the sector with the Data Address mark and reads the next sector

Read A Track

This command is similar to the Read Data command except that this is a continuous Read operation where the entire data field from each of the sectors is read. Immediately after sensing the index hole, the FDC starts leading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and sets the ND flag of status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT If the FDC does not find an ID Address mark on the diskette after it senses the index hold for the second time, it sets the MA (Missing Address mark) flag in Status Register 1 to a 1 (high) and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

Read ID arms to as (right) 1 a of the laips 9 autot3

The Read ID command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address mark is found on the diskette before the index hole is encountered for the second time, then the MA (Missing Address mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format A Track

The Format command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; Gaps, Address marks, ID fields and data fields, all per the IBM System 34 (double density) or System 3740 (single density) format are recorded. The particular format which will be written is controlled by the values programmed inlo N (number ot bytes/sector), SC (sectors/cylinder), GPL (gap length), and D (data pattern) which are supplied by the processor during the Command phase. The data field is filled with the byte of data stored in D. The ID field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (cylinder number), H (head number), R (sector number) and N (number of bytes/sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the ST37C65 for each sector on the track. If FDC is set for the DMA mode, it will issue four DMA requests per sector. If it is set for the Interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R register are incremented by 1 after

each sector is formatted; thus, the R register contains a value of R when it is read during the Result phase. This incrementing and formatting continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

Table 33 shows the relationship between N, SC, and GPL for various sector sizes.

TABLE 33. N, SC AND GPL RELATIONSHIP

FORMAT	SECTOR SIZE	N	sc	GPL1	GPL2,3
8" STANDA	ARD FLOPPY			2 918 1	101914
FM MODE					
	128 bytes/sector	00	1A	07	1B
	256	01	OF	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM	256	01	1A	0E	36
selles edd	512	02	OF	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	- 06	01	C8	FF
CERTIFICA	Julia of Sept	590-017	SHIW	UEL SITE	I en
5 1/4" MINI FM MODE	-FLOPPY				
FIVI WODE	128	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM MOD	En UEDG online				
	256	01	12	OA	OC
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	FO
	2048	04	02	C8	FF
	4096	05	01	C8	FF
	Y MICRO-FLOPPY	Lit bah	anima	nd is te	smirto
FM MODE					
	128	00	OF	07	1B
	256	01	09	0E	2A
	512	02	05	1B	ЗА
MFM MOD	E askeyo oh a				
	256	01	OF	0E	36
	256	02	09	1B	54
	1024	03	05	35	74
	1024	03	03	33	14

Scan Commands

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meets the condition of the comparison. Ones complement arithmetic is used for comparison (FF=largest number, 00=smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP -8R), and the scan operation is continued. The scan operation continues until one of the following conditions occur the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met, then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high) and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Regisler 2 is a 1 (high) and terminates the Scan command. The receipt of a Terminal Count signal from the processor or DMA controller durring the scan operation will cause the FDC to complete the comparison of the particular byte which is in process and the to terminale the command. Table 34 shows the status of bits SH and SN under various conditions of Scan.

TABLE 34. STATUS OF BITS SH AND SN

COMMAND	BIT-2	BIT-3	COMMENTS
Scan Equal	0	19000	DFDD = Dprocesso
	1	0	DFDD ≠ Dprocesso
	0	an 1 avn	DFDD = Dprocesso
Scan Low		0	DFDD < Dprocesso
or Faulal	ulvo 1	0	DFDD > Dprocesso
	U	1	DFDD = Dprocesso
Scan High	0	0	DFDD > Dprocesso
or Equal	1	0	DFDD < Dprocesso

If the FDC encounters a Deleted Data Address mark on one of the sectors (and SK=0), then it regards the sector as the last sector on the cylinder, sets the CM (Control mark) flag of Status Register 2 to a 1 (high) and terminates the command If SK=1, the FDC skips the sector with the Deleted Address mark and reads the next sector. In the second case (SK=1), the FDC sets the CM (ConIrol mark) flag of Status Register 2 to a 1 (high) in order to show that a deleted sector had been encountered.

When either the STP (contiguous sectors=01, or alternate sectors=02) sectors are read or the MT (Multitrack) is programmed it is necessary to remember that the last sector on the track must be read. For example, if STP=02, MT=0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sertor 21, the following will happen: sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the index hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

During the Scan command, data is supplied by either the processor or DMA controller for comparison against the data read from the diskette. In order to avoid having the OR (Overrun) flag set in Status Register 1, it is necessary to have the data available in less than $27\mu s$ (FM mode) or $13\mu s$ (MFM mode). If an Overrun occurs, the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

Seek

The Read/Write head within the FDD is moved from cylinder to cylinder under control of the Seek command. FDC has four independent Present Cylinder Registers for each drive. They are cleared only after the Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if Ihere is a difference, performs the following operations:

PCN < NCN: Direction signal to FDD set to a 1 (high), and step pulses are issued. (Step In)

PCN > NCN: Direction signal to FDD set to a 0 (low), and step pulses are issued. (Step Out)

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued NCN is compared against PCN, and when NCN = PCN, lhe SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated At this point FDC interrupt goes high. Bits D0B-D3B in the Main Status Register are set during the Seek operation and are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the FDC is in the FDC Busy state; but during the Execution phase, it is in the non-busy state. While the FDC is in the non-busy state, another Seek command may be issued, and in this manner parallel Seek operalions may be done on up to four drives at once. No other command can be issued as long as the FDC is in the process of sending step pulses to any drive.

If the time to write three bytes of Seek command exceeds 150µs, the timing between the first two step pulses may be shorter than that set in the Specify command by as much as 1ms.

Recalibrate

The function of this command is to retract the Read/ Write nead within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and step pulses are issued. When the Track 0 signal goes high, the SE (Seek End) flag in Status Register 0 is set to a 1 (high) and the command is terminated If the Track O signal is still low after 255 step pulses have been issued, the FDC sets the SE (Seek End) and EC (Equipment Check) flags of Status Register 0 to both 1s command after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the Ready signal, as described in the Seek command, also

Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following reasons:

- 1 Upon entering the Result phase of
- Read Data command
- Read A Track command
- · Read ID command
- Read Deleted Data command
- Write Data command
- Format A Cylinder command
- Write Deleted Data command
- · Scan commands
- 2 Ready Line of FDD changes state
- 3 End of Seek or Recalibrate command
- 4 During Execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor During an Execution phase in non-DMA mode, DBS in the Main Status Register is high. Upon entering the Result phase, this bit gets cleared. Reasons 1 and 4 do not require Sense Interrupt Status commands.

The interrupt is cleared by Reading/Writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status command. This command, when issued. resets the Interrupt signal and via bits 5, 6, and 7 ot Status Register 0 identifies the cause of the interrupt.

TABLE 35. INTERRUPT CAUSE

BIT-5	BIT-6	BIT-7	CAUSE
0	1	1	Ready line changed state, either polarity.
1	0	0	Normal Termination of Seek or Recalibrate command.
1	1	0	Abnormal Termination of Seek or Recalibrate command.

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no Result phase. When the disk drive has reached the desired head position, the ST37C65 will Set the Interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives. See Figure 7.

The Specify command sets the initial values for each of the three internal timers: The HUT (Head Unload Time) defines the time from the end of the Execution phase of one of the Read/Write commands to the head unload state Thistimer is programmable from 16 to 240ms in increments of 16ms (01=16ms, 02=120ms, 0F=240ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16ms in increments of 1ms (F=1ms, E=2ms, D=3ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the Read/Write operation starts. This timer is programmable from 2 to 254ms in increments of 2ms (01=2ms, 02=4ms, 03=6ms . . . 7F=254ms).

The time intervals mentioned above are a dirert lunction of the clock (CLK on pin 23). Times indicated above are for a 16MHz clock; if the clock was reduced to 8MHz, then all time intervals are increased by a factor of 2. If the clock was increased to 32MHz, then all time in tervals are decreased by half.

The choice of DMA or non-DMA operation is made by the ND (Non-DMA) bit. When this bit is high (ND = 1), the Non-OMA mode is selected; and when ND = 0, the DMA mode is selected.

Sense Drive Status

This command may be used by the processor to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

Invalid

If an Invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set

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to 1 and 0 respectively. No interrupt is generated during this condition. Bits 6 and 7 (DIO and RQM) in the Main Status Register are both high (1), indicating to the processor that the ST37C65 is in the Result phase and the contents of Status Register 0 (STD) must be read When the processor reads Status Register 0, it will find an 80 hex, indicating an Invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt; otherwise the FDC will consider the next command to be an invalid command. In some applications, the user may wish to use this command as a No-Op command to place the FDC in a standby or No Operation state.

FIGURE 8. ST37C65 FM MODE FORMAT

GAP	SYNC	IAM	GAP	SYNC	IDAM	C	Н	S	N	C	GAP	SYNC	DATA	DATA	С	GAP	GAP
(4a)	6x	FC	(1)	6x	TFE .	Y	D	E	0	R	(2)	6x	AM	s F and	R	(3)	(4b)
40x	00	is rig	26x	00	à bso.	be	9HI	C	eriv	C	11x	00	FB	pilerage	C	nsam	roo h
FF	metod	no ai	FF	This	etrole	KION	physic	20 5	tinta		FF	Execu	or	sor the	29	Scari I	orft v
	100 m	erC 32	- street	manna	F 61 64	20.00	3 0	10			one has	S reled	F8	-oun		man I	2.857

FIGURE 9. ST37C65 MFM MODE FORMAT

GAP (4a) 80x	SYNC 12x 00	IAM 3x C2	GAP (1) 50x	SYNC 12x 00	IDAM 3x A1	CYL	НД	SEC	0 2	CRC	GAP (2) 22x	SYNC 12x 00	DATA AM 3x	DATA	CRC	GAP (3)	GAP (4b)
FF	SZMHU	FC	4E	Mas in	FE	eru	2.1	to N	acti		4E	ense	A1 FB		ru	w ba	
		Men I	0 000	85108	916 2		3616	911	12 116		.bou	szi nen	F8	rimos		bas	

BIT-5 BIT-6 BIT-7 CAUSE

0 1 1 Ready line changed state, either polarity.

1 0 0 Morrai Termination of Seek or Recalibrate command.

1 1 0 Abnormal Termination of Seek of Recalibrate seek of Recalibrate command.

AC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Limits Typ	Max	Units	Condi	tions
T,	Clock high pulse duration Clock low pulse duration	13.5 13.5	TICS	TERB	ns	TRICAL C	C ELEC
T 2	Clock rise/fall time	10.0		2	ns		
T ₂ T ₃ T ₄		0	therwise	unless o		C, Voc=5.0	=Q° - 70°
T,	RD* width	90			ns		
T ₅	A0, CS*, DACK* hold time to RD* high	0		rot	ns		
T ₈	Data access time from RD* low			90	ns		
T ₉	Data bus to float delay from RD* high	10		65	ns	I wol tugni	
T ₁₀	IRQ reset delay time from RD* high	2.3		T ₁₈	ns	+150ns	
T ₁₁	A0, CS*, DACK*, LDCR*, LDOR* set up time to WR* low	0		DX, IRG	ns	Output low DMA	
T ₁₂	WR* width	60	1	Dx, IRd	ns	Output hig	
1 13	A0, CS*, DACK*, LDCR*, LDOR* hold time from WR* high	0		ine	ns mus doin	DMA Output low	Vацис
T ₁₅	Data set up time to WR* high	80			ns	open drain	
T.,	Data hold time from WR* high	0		Insur	ns	Avg. power	
1,7	IRQ reset delay time from WR* high			T ₁₈	ns	+150ns	
140	DMA cycle time	52			T ₁₈ 90	Input leaks	
T,0	DACK* delay time from DMA high	0		Schmitt	ns	Input low 1	
T ₂₀	DMA reset delay time from DACK* low	14	1	140	ns	Input high	
104	DACK* width	90		risis	ns	Schmitt tri	
T ₂₂	RD* or WR* response from DMA high			48	T ₁₈		
723	RD* delay from DMA	0			ns		
T	WR* delay from DMA	0			ns		
T ₂₈	TC delay from last DMA or IRQ, RD*	0		192	T ₁₈		
1 20	TC delay from last DMA or IRQ, WR*	0		384	T ₁₈		
T ₃₀	TC width	60			ns	AHYG	
31	Reset width - TTL driven CLK1	60			ns		
1 32	Chip access delay from RST low	32			ST T ₁₈		
T ₃₃	DIRC* hold & set up to STEP* low	4	- 1	100	T ₁₈		
34	STEP* active time low	24			T ₁₈	1	
35	DIRC* hold time after STEP*	96			T ₁₈		
T ₃₆	STEP* cycle time	132			T ₁₈		
27	DSX* hold time from STEP* low	20			T ₁₈		
38	IDX* index pulse width	2	-		T ₁₈		
39	RDD* active time low	40	010	dor	ns	0	
T ₄₀	WD* write data width low		1/2		WCLK	HELL AND THE	

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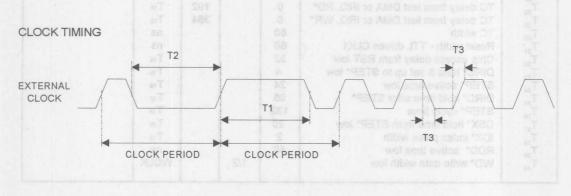
ABSOLUTE MAXIMUM RATINGS

Supply range Voltage at any pin Operating temperature Storage temperature Package dissipation 7 Volts GND-0.3 V to VCC+0.3 V 0° C to +70° C -40° C to +150° C 500 mW

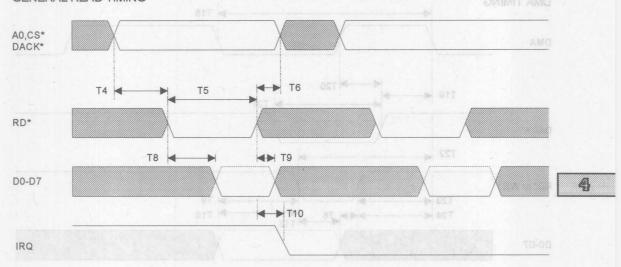
DC ELECTRICAL CHARACTERISTICS

 $T_A=0^{\circ}$ - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

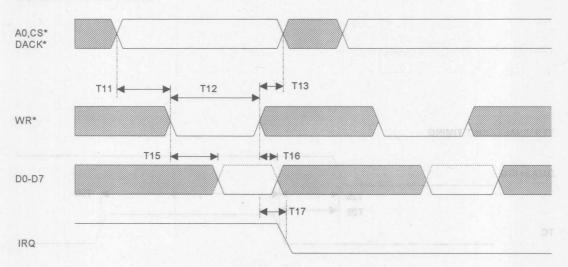
Symbol	Parameter	Min	Limits Typ	Max	Units	Conditions
V _{IL}	Input low level	-0.5		0.8	V	Data accel
VIH	Input high level	2.2	dest YO	VCC	V	distance (CE)
V _{IH} V _{OL}	Output low level for Dx, IRQ, DMA	0 1	*80	0.4	V	I _{oL} = 24 mA
V _{OH}	Output high level for Dx, IRQ, DMA	2.8	*808	ar van	V	I _{OH} = -5 mA
V _{OLHC}	Output low-high current open drain		-	0.4	V	I _{oL} = 24 mA
I _{cc}	Avg. power supply current		5	DE-SUA/	mA	Plantataria
Iccc	Power down current		100	W mord	μΑ	tess 091
	Input leakage	l la		±10	μΑ	Mayo AMO
I _{IL} V _{ILT}	Input low trashold - "Schmitt"	0.8	dpid A	1.1	V	NACIONE
VIHT	Input high trashold - "Schmitt"	1.7	ACIC!	2.0	V	Pages Aldin
V _{HYS}	Schmitt trigger hysterisis	0.45	OH AND	about a	V	DACK* WIL

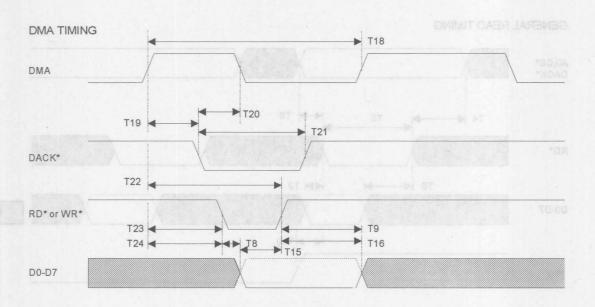


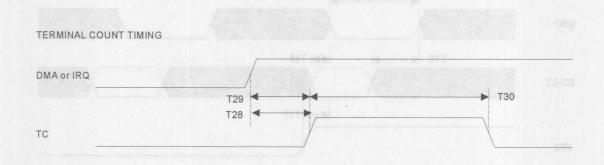




GENERAL WRITE TIMING

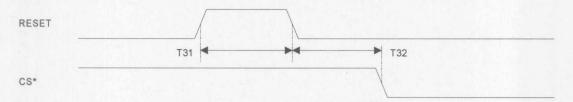






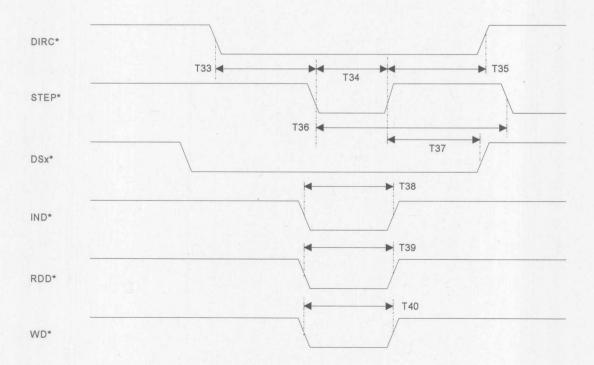
GENERAL WRITE TIMING

RESET TIMING



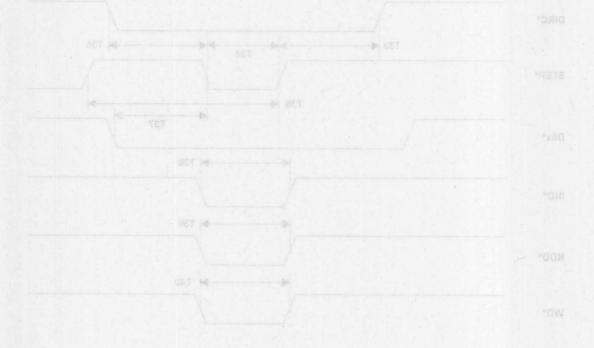
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DISK DRIVE TIMING









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PRODUCTS PREVIEW

BLOCK DIAGRAM

Printed September 8, 1994

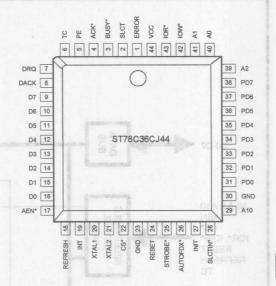
ECP/EPP PARALLEL PRINTER PORT WITH 16 BYTE FIFO

DESCRIPTION

The ST78C36 is a monolithic Bidirectional ECP/EPP Parallel port designed to operate as a general purpose I/O port. It contains all the necessary input/output signals to be configured as a CENTRONICS printer port, MicroSoft/HP ECP, IBM EPP smart printer port. The ST78C36 is a general purpose input/output controller with 16 byte internal FIFO. FIFO operation can be enabled or disabled. For CENTRONICS printer operation, all registers are mapped to IBM printer port registers.

The ST78C36 is designed to operate as normal printer interface without any additional settings.

PLCC Package



FEATURES

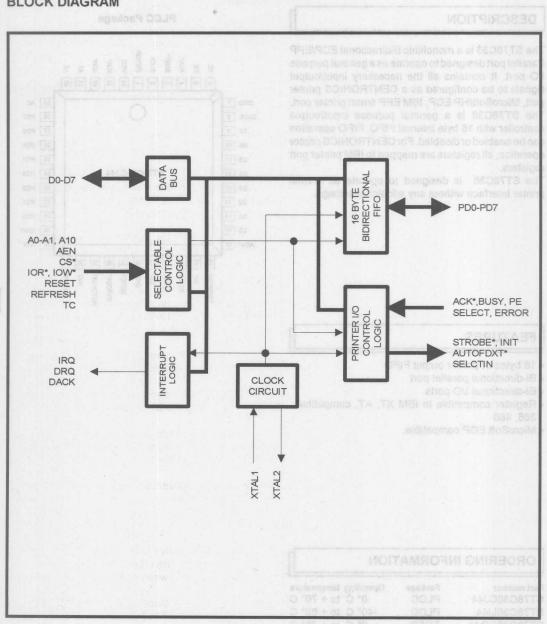
- 16 bytes of printer output FIFO
- · Bi-directional parallel port
- · Bi-directional I/O ports
- Register compatible to IBM XT, AT, compatible 386, 486
- · MicroSoft ECP compatible.

ORDERING INFORMATION

Part number	Package	Operating	temperature
ST78C36CJ44	PLCC	0° C	to + 70° C
ST78C36IJ44	PLCC	-40° C	to + 85° C
ST78C36CO48	TOFP	0° C	to + 70° C

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BLOCK DIAGRAM



Symbol	Pin	Signal Type	Pin Description
ERROR*	l clock can be	isoutt, via external suit and beud rate g	General purpose input or line printer error (active low). This is an output from the printer to indicate an error by holding it low during error condition.
SLECET WOLA		out 2 or buffered o	General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY*	niq sint no dok		General purpose input or line printer busy (active low). An output from the printer to indicate printer is not ready to accept data.
bliev that valid		uppose ^I I/O or dail . This culput indication in the product	General purpose input or line printer acknowledge (active low). This input is pulsed low by the printer to indicate that data has been accepted successfully.
printer should		urpose VO or auto	General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper.
niero nego) rai	d alize tine prin	illy line feed after uppose IAO or inflat. When this signed st.	Terminal Count (active high). This signal indicates to ST78C36 that data transfer is complete. If DMA operation mode is selected for command execution, TC will be qualified by DACK*, but not in the programmed I/O execution.
DRQ	inter select (o) it selects the	ronse I/O or line po titis sonal is low	Direct Memory Access Request (three state, active high). DMA request for byte transfers of data.
DACK*	internal region 8		DMA ACKNOWLEDGE (active low). Used by DMA controller to transfer data from the ST78C36 onto the bus.
D7-D0	9-16	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus.
		oe (active low). A to	Host address enable (active low). All decoded addresses are valid when AEN* is low.
REFRESH	18	(al. (wol a litos) so	Referesh cycle.
IRQ U90	19	te of the ST78C to	Printer interrupt output (active low). To signal the state of the printer port. This pin tracks the ACK* input pin, When ACK* is low IRQ is low and when ACK* is high IRQ is high
XTAL1	20	ply input	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal



"Have intental pull-up resistor on inputs

Symbol	Pin	Signal Type	Pin Description						
		irpose input or line it from the printer g error condition	I illerina di cuit and badd rate generator for custom transmis-						
XTAL2	toelee21 Ining	rpose liput or line output from the p	Crystal input 2 or buffered clock output. See XTAL1.						
CS*	22	been sylected.	Parallel printer port chip select (active low). A low at this pin enables the parallel port / CPU data transfer operation.						
		n the printer to in	Master reset. (active high) A high on this pin will reset all the outputs and internal registers.						
STROBE* Deland	by the printer	uposeopled such neur accepted such sen accepted such	General purpose I/O or data strobe output (open drain active low). This output indicates to the printer that valid data is available at the printer port (PD0-PD7).						
door of paper.		apose of put ar ting the principut from the principut Count (active in	General purpose I/O or automatic line feed (open drain active low). When this signal is low the printer should automatically line feed after each line is printed.						
DMA operation	s co* ₂₇ * oo z fuoexe brien		General purpose I/O or initialize line printer (open drain active low). When this signal is low, it causes the printer to be initialized.						
SLCTIN*		OVI nory Access Related for byte transfer	General purpose I/O or line printer select (open drain active low). When this signal is low, it selects the printer.						
A10	29	NOWLEDGE (adit	Address select line. To select internal registers.						
PD0-PD7 ^d ent of sud state data bus to	31-38 TE onto	fer da on the nel data bus. Eigh	Bi-directional parallel ports (three state). To transfer data in or out of the ST78C36 parallel port. PD7-PD0 are latched during output mode.						
A0-A2	39-41	bit of the data bu	Address select lines. To select internal registers.						
iow***bbs bebo	osb II42(wot	ess enable (activitien then AEN* is low	Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register.						
IOR*	43	yde. 1	Read strobe (active low). A low level on this pin transfers the contents of the ST78C36 data bus to the CPU.						
GNDV nig tug	23,30	port, Toe pin the port of the	Signal and power ground.						
DOV	44	o lansette to t his	Power supply input.						

^{*} Have internal pull-up resistor on inputs

INTRODUCTION

This parallel interface is designed to provide all of the signals and registers needed to communicate through a standard parallel printer port as found in the IBM PC, AT, PS/2 and Centronics systems. The address decoding of the registers utilizing A0, A1 and A10 is

shown in Table 1. All bits in these registers are located in the same positions and have the same functions as the registers of the systems listed above.

NAME	ADDRESS	R/W	SIZE	MODE	FUNCTION
DATA	Port+0 Hex	R/W	byte	000	Data Register
DATA	Port+0 Hex	R/W	byte	001	Data Register
AFIFO	Port+0 Hex	R/W	byte	011	ECP FIFO
STR	Port+1 Hex	R	byte	ALL	Status Register
CTR	Port+2 Hex	R/W	byte	ALL	Control Register
CFIFO	400 Hex	R/W	PWord	010	Parallel Port Data FIFO
DFIFO	400 Hex	R/W	PWord	011	ECP FIFO
TFIFO	400 Hex	R/W	PWord	110	Test FIFO
CNFGA	400 Hex	R/W	byte	111	Configuration Register A
CNFGB	401 Hex	R/W	byte	111	Configuration Register B
ECR	402 Hex	R/W	byte	ALL	Extended Control Register

REGISTER DEFINITIONS

DATA REGISTER (Mode 000, 001)

This is a bi-directional data port that transfers 8-bit data to or from PD7-0. The CTR-5 bit will determine the data direction in conjunction with the Read and Write strobes.

AFIFO (Mode 011)

ECP Add FIFO register. Write only. In the forward direction a byte written into this register is pushed into the FIFO and tagged as a ECP Address / RLE command. Reading this register has no effect and the data read is undefined. Writes to this register during backward direction have no effect and the data is ignored.

Bit-7:

1 = AFIFO bits 0-6 are ECP address.

0 = AFIFO bits 0-6 is a run length (RLE), indicating how many times the next data byte is to appear.

000000 = 1 time.

000001 = 2 time.

000010 = 3 time.

and so on.

Bit 0-6: 9 Teleng eff. ("XOA) langle agbetwonxis

Address or RLE fields.

STATUS REGISTER

This register provides status for the signals listed below. It a read only register. Writing to it is an invalid operation that has no effect.

Bit-0: oldered accept and reflere Characterist

When in EPP mode, this is the time-out status bit. When this bit is "1", time-out occurred on EPP cycle (min. $10\mu s$). It is cleared to "0" after STR is read. Consecutive reads(after the first read) always return "0". It is also cleared to "0" when EPP is enabled. When not in EPP mode, this bit is "1".



in the same positions and have the same fund; 1-till

Reserved, this bit is always "1".

Bit-2

In the compatible mode, or in ECP and EPP mode with bit-4 of PCR = 0, this bit is always "1". In the Extended Mode (PTR-7 bit is "1"), or in ECP and EPP with bit-4 of PCR = 1 this bit is the status bit. In the Extended mode, If CTR-4 = 1, then this bit is latched low when the ACK* signal makes a transition from low to high. Reading this bit sets it to a "1".

Bit-3:

This bit represents the current state of the printer error signal. The printer sets this bit low when there is a printer error. This bit follows the state of the error pin.

Bit-4:

This bit represents the current state of the printer select signal (SLCT). The printer sets this bit high when it is selected. This bit follows the state of the SLCT pin.

Bit-5:

This bit represents the current state of the printer paper end signal (PE). The printer sets this bit high when it detects the end of the paper. This bit follows the state of the PE pin.

Bit-6:

This bit represents the current state of the printer acknowledge signal (ACK*). The printer pulses this signal low after it has received a character and is ready to receive another one. This bit follows the state of the ACK* pin.

Bit-7

:This bit represents the current state of the printer BUSY* signal. The printer sets this bit low when it is BUSY* and cannot accept another Characters. This bit is the inverse of the (BUSY*) pin.

CONTROL REGISTER

This register provides all output signals to control the printer. Except for bit-5, it is a read and write register.

Normally when the Control Register is read, the bit values are provided by the internal output data latch. These bit values can be superseded by the logic level of the STROBE*, AFD*, INIT, and SLIN* pins, if These pins are forced high or low by an external voltage. In order to force these pins high or low the corresponding bits should be set to their Inactive state.

Bit-0:

This bit directly controls the data STROBE* signal to the printer via the STROBE* pin. This bit is the inverse of the pin.

Bit-1:

This bit directly control the automatic feed XT signal to the printer the AFD* pin. Setting this bit high causes the printer to automatically feed after each line is printed. This bit is the inverse of the AFD* pin.

Bit-2

This bit directly controls the signal to initialize the printer via the INIT pin. Setting this bit to low initializes the printer. This bit follows the INIT signal pin.

Bit-3:

This bit directly controls the select in signal to the printer via the SLIN* pin. Setting this bit high selects the printer. It is the inverse of the SLIN* pin.

Bit-4:

This bit enables the parallel port interrupt. Setting this bit low puts IRQ into THREE-STATE and clears any pending interrupts. In the AT Compatible Mode, or in EPP or ECP modes when this bit is set high, the IRQ signal follows the ACK* signal transitions (pulse interrupt). In the Extended Mode, or in either EPP or ECP modes when this bit is set high, The IRQ signal should set high on the low to high transition of the ACK* signal.

Bit-5:

This bit determines the parallel port direction. The default condition results in the parallel pin being in the output mode. This is a Read/Write bit in EPP mode. In compatible mode it is a write only bit; a read from it will return "1".

Bits 6-7:nep citamotus, and suits full bits vigine

Reserved. These bits are always.

CFIFO (Mode 010) gnibnagxa (BUR) gnibeonal

Parallel Port FIFO Register. Write only. A byte written, or DMA-ed, to this registers pushed into The FIFO and tagged as data. Reading this register has no effect and the data read is undefined.

DFIFO (Mode 011)

ECP Data FIFO Register. In the forward direction a byte written, or DMA-ed, to this register is pushed into the FIFO and tagged as data. Reading this register has no effect and the data read is undefined. In the backward direction the ECP automatically issues ECP read cycles to fill the FIFO. Reading this register pops a byte from the FIFO. Writing this register has no effect and the data written is ignored.

TFIFO (Mode110) and beautiful as AMO narthy

Test FIFO Register. A byte written into this register is pushed into the FIFO. A byte read from this register is popped from the FIFO The ECP does not issue a ECP cycle to transfer the data to or from the peripheral device. The TFIFO is readable and writ able in both directions. In the forward direction PD7-0 is driven, but the data is undefined. The FIFO does not stall when overwritten or under-run (access is ignored). Bytes are always read from the top of the FIFO, regardless of the direction bit.

CNFGA(Mode 111) THE BATT bendebtor at stab been

Configuration Register A. Read only. Reading this register always returns 10Hex. Writing this register has no effect and the data is ignored.

CNFGB (Mode111) nonpi ai nettiny stab ,benitobnju

Configuration Register B. Read only. Reading this register returns the configuration parallel port interrupt line, and its state.

To improve noise immunity in ECP cycles, The RDA

Extended Control Register. This register controls the ECP and parallel port functions. Upon reset this register is Initialized to 16Hex.

Bit 5-7:

ECP DMA Enable bit. When this bit is :000 aboM

Standard mode. Write cycles are performed under software control. Bit-5 of CTR is forced to "0" and PD7-0 is driven. The FIFO is reset (empty).

Mode 001:

PS/2 mode. Read and write cycles are performed under software control. The FIFO is reset.

Mode 010:

Parallel Port FIFO mode. Write cycles are performed under hardware control (STROBE* is controlled by hardware). Bit-5 of CTR is forced to "0" and PD7-0 are driven.

Mode 011: and of salved short no triple are shart

ECP FIFO mode. The FIFO direction is controlled by bit-5 of CTR. Read and write cycle to the device are performed under hardware control (STROBE* and AFD* are controlled by hardware).

Mode 100:

Reserved

has at least one free byte. This pit is "I" wi:101 aboM

Reserved. and alositer ylaununitnoo lid aid? alut ai

is ignored. When the ECP clock is stopp:110 aboM.

FIFO test mode. The FIFO is accessible via the TFIFD register. The ECP does not issue ECP cycles to fill/empty the FIFO.

FIFO has at least one byte of data. This bit 1 show

Configuration mode. The CNFGA and CNFGB registers are accessible in this mode.

Bit-4: art to easily spen "1" as been at tid airt, beggota

ECP Interrupt Mask bit. When this bit is "0" an interrupt is generated on ERROR assertion. An interrupt is also generated when ERROR is asserted while this bit is changed from "1" to "0"; this prevents the loss of an interrupt between ECR read and ECR write. When this bit is "1", no interrupt is generated.



Bit-3:

ECP DMA Enable bit. When this bit is "0", DMA is disabled and the PDRQ pin is in TRI-STATE. When this bit is "1", DMA is enabled and DMA starts when bit-2 of ECR is "0".

Bit-2:

ECP Service bit. When this bit is "0", and one of the following three interrupt events occur, an interrupt is generated and this bit is set to "1" by hardware.

- Bit-9 of ECR is "1", and terminal count is reached during DMA.
- Bit-3 of ECR is "0" and bit-5 of CTR is "0", and there are eight or more bytes free in the FIFO.
- c. Bit-3 of ECR is "0" and bit-5 of CTR is "1", and there are eight or more bytes to be read from the FIFO. When this bit is "1", DMA and the above three interrupts are disabled. Writing "1" to this bit does not cause an interrupt. When the ECP clock is stopped this bit is read as "0", regardless of its actual value.

Bit-1:

FIFO Full bit. Read only. This bit is "0" when the FIFO has at least one free byte. This bit is "1" when the FIFO is full. This bit continuously reflects the FIFO state, and therefore can only be read. Data written to this bit is ignored. When the ECP clock is stopped the bit is read as "1", regardless of the actual FIFO state.

Bit-0:

FIFO Empty bit. Read only. This bit is "0" when the FIFO has at least one byte of data. This bit is "1" when the FIFO is empty. This bit continuously reflects the FIFO state, and therefore can only be read. Data written to this bit is ignored. When the ECP clock is stopped, this bit is read as "1", regardless of the actual FIFO state.

EXTENDED CAPABILITIES PARALLEL PORT

The ECP support includes a 16-byte FIFO that can be configured for either direction, command / data FIFO, a FIFO threshold interrupt for both directions, FIFO

empty and full status bits, automatic generation of strobes (by hardware) to fill or empty the FIFO, transfer of commands and data, and a Run Length Encoding (RLE) expanding /decompression) as explained below.

The Extended Capabilities Port (ECP) is enabled when bit-2 of PCR is "1". Once enabled, its mode is controlled via the mode field of ECR-bits 5, 6, 7 of ECR register.

The ECP has ten registers:

The AFIFO, CFIFO, DFIFO and TFIFO registers access the same ECP FIFO. The FIFO is accessed at Base + 000Hex, or Base + 400Hex, depending on the mode field of ECR and the register. FIFO can be accessed by host DMA cycles, as well as host PIO cycles.

When DMA is configured and enabled (bit-3 of ECR is "1" and bit-2 of ECR is "0") the ECP automatically issues DMA requests to fill the FIFO (in the forward direction when bit-5 of CTR is "0") or to empty the FIFO (in the backward direction when bit-5 of CTR is "1"). All DMA transfers are to or from these registers. The ECP does not assert DMA request for more than 32 consecutive DMA cycles. The ECP stops requesting DMA when TC is detected during an ECP DMA cycle.

Writing into a full FIFO, and reading from an empty FIFO, are ignored. The written data is lost, and the read data is undefined. The FIFO empty and full status bits are not latched by such access. Some registers are not accessible in all modes of operation, or may be accessed in one direction only. Accessing a non-accessible register has no effect: Data read is undefined, data written is ignored, the FIFO does not update. The ST78C36 Parallel Port registers (DTR, STR and CTR) are not accessible when ECP is enabled.

To improve noise immunity in ECP cycles, The state machine does not examine the control handshake response lines until the data has had time to switch.

The software should enable ECP after bits 0-

3 of the parallel port control register (CTR) are "0".

- b. When ECP is enabled, and the software wishes to switch modes, it should switch only through modes 000 or 001.
- When ECP is enabled, The software should change direction only in mode 001.
- d. The software should switch from mode 010, or 011, to mode 000, or 001, only when the FIFO is empty.
- e. The software should switch to mode 011 when bits 0,1 of CTR are "0".
- f. The software should switch to mode 010 when bit-0 of CTR is "0".
- g. The software should disable ECP only when in mode 000 or 001.

Software may switch from mode 011 backward direction to modes 000 or 001 when there is an ongoing ECP read cycle. In this case the read cycle is aborted by deasserting AFD*. The FIFO is reset and a potential byte expansion is automatically terminated since the new mode is 000 or 001.

The ECP uses the Xtal1 clock. This clock can be stopped for power down mode. When this power-down mode occurs, the DMA is disabled, all interrupts (except ACK*) are masked, and the FIFO registers are not accessible. The other ECP registers are always accessible when the ECP is enabled. During this period the FIFO status and contents are not lost, although the host reads bit-2 of ECR as "0", bit-1 of ECR as "1" and bit-0 of ECR as "1", regardless of the actual values of these bits. When the clock starts toggling again these bits resume their original functions.

When the clock is stopped, an on going ECP cycle may be corrupted but the next ECP cycle will not start even if in forward direction the FIFO is not empty, and in backward direction the FIFO is not full. If the ECP clock starts or stops toggling during a host cycle that

accesses the FIFO, the cycle may yield wrong data.

SOFTWARE CONTROLLED DATA TRANSFER (MODES 000 AND 001)

Software controlled data transfer is supported in modes 000 and 001. The software generates peripheral device cycle by modifying the DATA and CTR registers and reading the STR, CTR and DATA registers. The negotiation phase and nibble mode transfer, as defined in the IEEE 1284 standard, are performed in these modes. In these modes the FIFO is reset and is not

Mode 000 is for the forward direction only; the direction bit is forced to "0" and PD7-0 is driven. Mode 001 is for both the forward and backward directions. The direction bit controls whether PD7-0 are driven.

AUTOMATIC DATA TRANSFER (Modes 010 and 011)

Automatic data transfer (ECP cycles generated by hardware) is supported only in modes 010 and 011. Automatic DMA access to fill or empty the FIFO is supported in modes 010, 011 and 110. Mode 010 is for the forward direction only; the direction bit is forced to "0" and PD7-0 is driven. Mode 011 is for both the forward and backward directions. The direction bit controls whether PD7-0 is driven.

Automatic Run Length Expanding (RLE) is supported in the backward direction.

Forward Direction (Bit-5 of CTR = 0)

When the ECP is in forward direction and the FIFO is not full

(bit-1 of ECR is "0") the FIFO can be filled by software writes to the FIFO registers (AFIFO and DFIFO in mode 011, and CFIFO in mode 010).

When DMA is enabled (bit-3 of ECR is "1" and bit-2 of ECR is "0") the ECP automatically issues DMA requests to till the FIFO with normal data bytes. When the ECP is in forward direction and the FIFO is not empty the ECP pops a byte from the FIFO write cycle to the peripheral device. The ECP drives AFD* according to the operation mode (ECR bits 5-7) and according to the tag of the popped byte as follows: In Parallel Port FIFO mode (mode 010) AFD* is



controlled by bit "1" of CTR. In ECP mode (mode 011) AFD* is controlled by the popped tag. AFD* is driven high for normal data byte and driven low for command byte.

ECP (Forward) Write Cycle 00 bns 000 zebom

An ECP write cycle starts when the ECP drives the popped tag onto AFD* and popped byte onto PD7-0. When BUSY* is low the ECP asserts STROBE*. In 010 mode the ECP deasserts STROBE* to terminate the write cycle. In 011 mode the ECP waits for BUSY* to be high. When BUSY* is high the ECP deasserts STROBE* and changes AFD* and PD7-0 only after BUSY* is low.

Backward Direction (Bit-5 of CTR is "1")

When the ECP is in the backward direction, and the FIFO is not full (bit-1 of ECR is "0"), the ECP issues a read cycle from the peripheral device and monitors the BUSY* signal. If BUSY* is high the byte is a data byte and it is pushed into the FIFO. If BUSY* is low the byte is a command byte.

The ECP checks bit-7 of the command byte, if it is high the byte is ignored, if it is low the byte is tagged as an RLC byte (not pushed into the FIFO but used as a Run Length Count to expand The next byte read). Following an RLC read the ECP issues a read cycle from the peripheral device to read The data byte to be expanded. This byte is considered a data byte, regardless of its BUSY* state. This byte is pushed into the FIFO (RLC+ 1) times.

When The ECP is in the backward direction, and the FIFO is not empty (bit-0 of ECR is "0"), the FIFO can be emptied by software reads from the FIFO register (only DFIFO in mode 011, no AFIFO and CFIFO read). When DMA is enabled (bit-9 of ECR is "1" and bit-2 of ECR is "0") the ECP automatically issues DMA requests to empty the FIFO (only in mode 011).

ECP (Backward) Read Cycle

An ECP read cycle starts when the ECP drives AFD* low. The peripheral device drives BUSY* high for a normal data read cycle, or drives BUSY* low for a command read cycle, and drives the byte to be read

onto PD7-0.

When ACK* is asserted the ECP drives AFD* high then reads the PD7-0 byte. When AFD* is high the peripheral device deasserts ACK* and may change BUSY* and PD7-0 states in preparation for the next cycle.

FIFO TEST ACCESS (MODE 110)

Mode 110 is for testing the FIFO in PIO and DMA cycles. Both read and write operations (pop and push) are supported, regardless of the direction bit. In the forward direction PD7-0 are driven, but the data is undefined This mode can be used to measure the host ECP cycle throughput, usually with DMA cycles. This mode can also be used to check the FIFO depth and its interrupt threshold, usually with PIO cycles.

CONFIGURATION REGISTERS ACCESS (MODE 111)

The two configuration registers, CNFGA and CNFGB, are accessible only in this mode.

Interrupt and short most doslike vem erswing?

Interrupt is generated when any of the following events occur.

- a. When bit-2 of ECR is "0", bit-3 of ECR is "1" and TC is asserted during the ECP DMA cycle.
- b. When bit-2 of ECR is "0", bit-3 of ECR is "0", bit-5 of CTR is "0" and There are eight or more bytes free in the FIFO. It includes the case when bit-2 of ECR is cleared to "0" and there are already eight or more bytes free in the FIFO (modes 010, 011 and 110 only).
- c. When bit-2 of ECR is "0", bit-3 of ECR is "0", bit-5 of CTR is "1" and there are eight or more bytes to be read from the FIFO. It includes the case when bit-2 of ECR is cleared to "0" and there are already eight or more bytes to be read from the FIFO (modes 011 and 110 only).
- d. When bit-4 of ECR is "0" and ERROR is asserted (high to low edge) or ERROR is asserted when bit-4 of ECR is modified from "1" to "0".
- e. When bit-4 of CTR is "1" and ACK* is deasserted (low-to-high edge). The interrupt is generated according to bits 4, 5 and 6 of PCR.

Special circuitry provides protection against damage that might be caused when the printer is powered but the ST78C36 is not.

Enhanced Parallel Port (EPP) modes of operation and one Extended Capabilities Port (ECP) mode to complete a full IEEE 1286 parallel port. In Compatible mode a write operation causes the data to be presented on pins PD7-0. A read operation In this mode causes the Data Register to present the last data written to it by the CPU.

In the Extended mode a write operation to the data register causes the data to be latched. If the Data Port Direction bit (CTR-5) is "0", the latched data is presented to the pins; if it "1" the data is only latched. When Data Port Direction bit (CTR-5) is "0", a read operation from this register allows the CPU to read the last data it written to the port. In the Extended Mode with the Data Port Direction bit set to "1" (read), a read from this register causes the port to present the data on pins PD7-0.



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Printed September 8, 1994

ADVANCED HIGH PERFORMANCE SUPER-I/O CONTROLLER

DESCRIPTION

The ST56C5XX is an advanced high performance super-I/O controller, designed to replace the IDE controller, four Floppy controllers, two serial ST16C550 UART's with advanced Microsoft/Hewlett Packard ECP, IBM EPP printer port and game port. The ST56C5XX utilizes digital phase locked loop for the floppy controller section to eliminate the external components (except the main crystal). The ST56C5XX is optimized for mother board applications as well as controller board applications. ST56C5XX provides high ESD circuits on the printer data bus and I/O to prevent damage caused by the printer being powered when the ST56C5XX is not powered.

FEATURES

- Licensed CMOS WD37C65C floppy controller.
- · Supports vertical recording format
- 100% IBM compatible
- · 48 mA drivers and schmitt Trigger inputs.
- DMA enable logic
- FDC primary and secondary address selection
- Two 16C550 serial ports
- Microsoft/Hewlett Packard Bi-directional ECP parallel port
- IBM EPP (Enhanced Printer Port)
- 16 bit IDE interface and decode logic
- Game port
- 100 pin TQFP and QFP packages
- Low power CMOS 1.2μ technology

ORDERING INFORMATION

Part number Package
ST56CXXXCQ100 QFP
ST56CXXXCTQ100 TQFP

Operating temperature 0° C to + 70° C 0° C to + 70° C s

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 - Game por
 - 100 pin TQFF and QFP packages
 - Low power CMOS 1.2 a technology

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Operating temperature 0°C to 4 70°C

0° C to + 70° C

GENERAL APPLICATION NOTE FOR STARTECH UART FAMILY

The AN-450 provides additional information to guide users to design or utilize the STARTECH product line. This document can also be used for all the STARTECH UART product lines.

GENERAL INFORMATION

STARTECH offers UART's with or without FIFO capabilities, and are marked as 45X for non FIFO families and 55X for FIFO families. All parts with sharing part numbers are foot print compatible in some extent, like ST16C450 and ST16C550, ST16C2450 and ST16C2550, etc.

This section will describe general terms for commonly used flags and registers.

OVERRUN ERROR:

The flag is set to "1" to warn the user that a serial data has been received and previous serial data has not been read from receive holding register. The new serial data will over write the previous data in the receive holding register. Note that previous serial data has been lost and user does not have an access to that data.

PARITY ERROR:

This flag is set "1" to indicate that received serial data contains mismatched parity or data bit error in the received data.

PARITY

Four common types of parities are used in the STARTECH Uart families; Odd Parity, Even Parity, Forced Mark Parity and Forced Space Parity.

ODD PARITY:

Odd Parity is calculated by adding all the "1's" in a data stream and adding a parity bit to the total bits, to make the total count an odd number.

Example -1: A data byte with the following pattern 11010010 will require to add a parity bit of "1" to bring the total count for "1's" to an odd number. Based on this data pattern, serial data with odd parity will be transmitted as 110100101.

Example -2: A data byte with the following pattern 10011000 will require to add a parity bit of "0" to maintain the total count of "1's" to an odd number.

Based on this data pattern, serial data with odd parity will be transmitted as 100110000.

EVEN PARITY:

Even Parity is calculated by adding all the "1's" in a data stream and adding a parity bit to the total bits, to make the count an even number.

Example -3: A data byte with the following pattern 10000101 will require to add a parity bit of "1" to bring the total count for "1's" to an even number. Based on this data pattern, serial data with even parity will be transmitted as 100001011.

Example -4: A data byte with the following pattern 00001111 will require to add a parity bit of "0" to maintain the total count for "1's" to an even number. Based on this data pattern, serial data with even parity, will be transmitted as 000011110.

FORCED SPACE PARITY:

Parity bit on the serial byte is set to "0" regardless of total number of "1's" (even or odd counts).

FORCED MARK PARITY:

Parity bit on the serial byte is set to "1" regardless of total number of "1's" (even or odd counts).

FRAMING ERROR:

The flag is set to "1" to indicate that received data does not have correct start or stop bits. This can cause when the Uarts are set for 8-bits word and receiving a serial data of 7-bits word or any mismatched data patterns.

BREAK SIGNAL INDICATION:

This flag is set to "1" to warn the user that transmitter is sending continuous "0" data without stop bit (RX input is low for more that one word).

TRANSMIT/RECEIVE FIFO:

STARTECH offers 16 byte transmit FIFO and 16 byte receive FIFO for all its products with 55X part numbers. These FIFO's are static 19 X 16 bit RAM with control logic to form a ring counter. Initializing the FIFO will set the write and read pointers to the same location.

TRANSMIT EMPTY:

This flag is set "1" to indicate that, there is no character in the transmit holding and transmit shift register

TRANSMIT HOLDING EMPTY:

This flag is set "1" to indicate that, there is one or more empty locations in the transmit holding register. User has to check this bit before loading characters in the transmit holding register. In non FIFO mode, user can load one character at a time when this flag is set and 16 characters when FIFO mode is utilized.

RECEIVER DATA READY:

This bit is set "1" to indicate that, receiver has one or more character in the receive holding register. User has to check this bit prior to read receive holding register. In non FIFO mode, only one character at time can be read. In FIFO mode up to 16 characters can be read if time bit is set.

RECEIVE TIME-OUT:

This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= 4 X P (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -7: If user programs the word length = 7, and no parity and one stop bit, Time out will be:

T = 4 X 7(programmed word length) +12 = 40 bits

Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -8: If user programs the word length = 7, with parity and one stop bit, the time out will be:

T = 4 X 7(programmed word length) + 12 = 40 bits

Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

BAUD RATE GENERATOR:

STARTECH provides a 16 bit digital divider to obtain all necessary baud rates. The 16 bit divider is broken down in to two 8-bit dividers which will be addressed as MSB divider (upper 8-bits) and LSB divider (lower 8-bits). To calculate the transmit/receive data rate it is necessary to know the provided clock rate (frequency) to STARTECH parts. STARTECH utilizes 16 clocks for each transmit bit and 16 clocks to sample the received data. Note that inorder to access these

dividers, user has to enable the divisor latch access bit through the Line Control Register.

Bit rate is calculated by:

Dividing decimal number = (Clock rate) / (16 X bit rate).

To program the digital divider, dividing decimal number should be converted to hex (base 16) number and split into two 8-bits sections.

Example -5: To obtain 4800 Hz baud rate, assuming 1.8432 MHz input clock, the dividing decimal value is (input clock=1843200) / (16 X 4800) = 24

24 decimal = 0018 Hex, this value is translated to MSB = 00 Hex and LSB = 18 Hex

BAUD RATE VERSUS BIT RATE:

The baud rate defines the width of each bit regardless of word, parity and stop bit length. Bit rate, is the rate of the transmission which each character is transmitted or received. The 2400 baud rate transmission is translated to 2400 Hz per bit for each character in a word. With 2400 baud you can transmit between 7 to 12 characters per slot.

PROGRAMMING STEPS:

The AN-450 provides the easy steps to program STARTECH Uart family. Note that all numbers are in Hex format not decimal.

Write 80 Hex to LCR (Line Control Register) to enable baud rate generator divider latch to set 2400 Hz baud rate:

write 00 Hex to MSB of baud rate generator (address location 1).

Write 30 Hex to LSB of baud rate generator (address location 0).

Select you word, parity and stop bit format from STARTECH Uart data sheet.

to set 8 bits, no parity and one top bit and disable the divisor access latch

write 03 Hex to LCR (Line Control Register):

if you need to use Uarts with FIFO, select your receive trigger level from data sheet.

to enable FIFO with 14 character trigger level write CF Hex to FCR (FIFO Control Register)

enable interrupt sources write 01 Hex to IER (Interrupt Enable Register) to select receive interrupt.

to set RTS and DTR outputs to low and enable the interrupt output write 0B Hex to MCR (Modem Control Register).

The STARTECH Uart is ready for transmit and receive operation.

Read MSR (Modern Status Register) to check the status of CD, RI, DSR, CTS input pins.

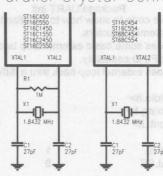
Read LSR (Line Status Register).

For polling applications (non interrupt mode) user has to monitor bit zero of this register to verify valid data in the receive holding register.

Check the Transmit Holding Empty bit before loading data in the transmit holding register,

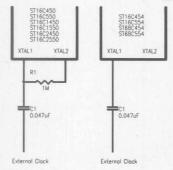
continue the transmission.

Parallel Crystal Connections

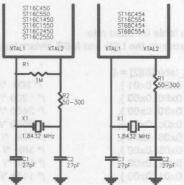


7/

External Clock Connections



Serial Crystal Connections



```
C PROGRAM SAMPLE
; File: sample.c
                       Package: UART init
 This is a sample code to show how to initialize the UART series of chips
; from Startech Semiconductors.
; This also includes some basic external loop back thru' two different bees well of eluquio STG bees STFI tax of
; ports using the FIFO capability.
; This also includes external loop back thru a different computer [21994] (OLINO) mebodi) HOM of xelf all allow
#include
             <stdio.h>
#include
             <string.h>
#include
             <fcntl.h>
#define
             TRUE
#define
             FALSE
                                       0
/* These are the various offsets for the registers inside the chip */
                                                                         For politing applications (non inter<sub>s</sub>upt
             RHR
                                       0x00 /* Receive Holding Register
                                                                          to monitor bit zero of this register.
#define
             THR
                                       0x00 /* Receive Holding Register
                                       0x01 /* Interrupt Enable Register */
#define
             IER
#define
             FCR
                                       0x02 /* FIFO control Register
                                                                          Check the Transmit Holding Empty
#define
                                       0x02 /* Interrupt Status Register
             ISR
                                                                       data in the transmit holding register /*
#define
             LCR
                                       0x03 /* Line control register
             MCR
                                       0x04 /* Modem Control Register
#define
#define
                                                                         */
             LSR
                                       0x05 /* Line Status Register
#define
             MSR
                                       0x06 /* Modem Status Register
#define
             SCR
                                       0x07 /* Scratch pad Register
                                                                          */
/* This two offsets are used for defining the baud rate
#define
             DIVLSB
                                       0x00 /* Divisor LSB latch address
#define
             DIVMSB
                                       0x01 /* Divisor MSB Latch address
 * Program table for baud rate
 * This represents the LSB and MSB divisor latch data
char baud_table[8][2] = {
          \{0x80, 0x01\},\
                                       /* 300 */
          0x60, 0x00 },
                                       /* 1200 */
          0x30, 0x00 },
                                      /* 2400 */
           0x0c, 0x00 },
                                       /* 9600 */
          0x06, 0x00 \},
                                      /* 19K */
          0x03, 0x00 \},
                                      /* 38k */
          \{0x02, 0x00\},\
                                      /* 56k */
         { 0x01, 0x00 }
                                      /* 115k */
};
```

```
/* Baud Rates */
#define
           COM_300
#define
           COM 1200
                                  1
                                  2
           COM 2400
#define
                                  3
#define
            COM 9600
            COM_19K
                                  4
#define
                                  5
           _COM_38K
#define
#define
           _COM_56K
                                  6
                                  7
#define
           COM 115K
/* Parity */
#define
           COM_NOPARITY
                                  0
#define
           _COM_ODDPARITY_
#define
           COM EVENPARITY
                                 2
/* Stopbits */
#define
            COM_STOP1_
                                  0
#define
           COM_STOP2
                                  1
#define
           COM_STOP1_5
                                  1
/* word length */
                                  0
#define
           _COM_CHR5_
#define
           _COM_CHR6
                                  1
                                  2
#define
           _COM_CHR7_
                                  3
#define
           _COM_CHR8_
/* word length */
#define
           _COM_FIFO1_
                                  0
#define
           _COM_FIFO4_
                                  1
#define
                                  2
           _COM_FIFO8_
                                  3
#define
           COM FIFO14
* This function checks the existence of a port.
* It is very simple. Take the port address then write to the scratch pad
* an the read it back. If the data read back the same as one that was
* written then return TRUE else return FALSE.
\*/
int
check_port(com_port)
int com_port;
{
 int i;
    printf("Checking for port %4xH\n",com port);
```

/* Write 1010 1010 (0xaa) to scratch pad*/

```
printf("Writing AAH in %4xH\n",com port);
 outportb(com port + SCR, 0xaa);
 /* read it back. If it the same then return TRUE */
 i = inportb(com_port + SCR);
   printf("Read back %2xH from %4xH\n",i,com_port);
 if(i == 0xaa)
      return TRUE;
  else
      return FALSE:
* This is the work horse function which actually setups the UART.
                                                                                 #define __COM_STOP1
* It needs to know every thing.
\*/
init_uart(port,baud,parity,data,stop,fifo,trigger)
int port, baud, parity, data, stop, fifo, trigger;
 char lcr byte;
 /* Set divisor latch */
 outportb(port+LCR, 0x80);
 printf("Divisor Latch is %2xH %2xH (High Low)\n",
                        baud_table[baud][1],baud_table[baud][0]);
 outportb(port+DIVLSB, baud table[baud][0]):
 outportb(port+DIVMSB, baud_table[baud][1]);
 /* Reset to normal Programming */
 /* Program the lcr_byte for the above parameters */
 Icr byte = 0x00;
 lcr_byte = data; /* Set the bit0 & bit1 for word length */
 Icr_byte ;= stop << 3; /* Set the bit2 for stop bit */
 if(parity != _COM_NOPARITY_) {
    Icr byte ;= 1 << 4; /* Set the bit3 for parity */
    if(parity == COM EVENPARITY )
      Icr byte := 1 << 5; /* Set the bit4 for EVEN parity */
 printf("LCR byte is %2xH\n",lcr_byte);
 /* Program LCR */
```

```
outportb(port+LCR, lcr_byte);
  if(fifo) {
   char fifo_byte;
   printf("Programming FIFOs without DMA mode\n");
   /* Have to first set the fifo enable */
   fifo byte = 0x01;
   outportb(port+FCR,fifo byte);
   /* Now program the FIFO */
   fifo_byte = 0x07; /* set bit0 - FIFO enable, Reset RCVR and XMIT FIFO */
   /* Program FCR */
   outportb(port+FCR,fifo byte);
   if(~(inportb(port + ISR) & 0xc0)) {
      printf("This port %4xH does not have FIFOs\n");
      printf("Hence did not program Enable FIFOs\n");
  /* Program IER */
  printf("Programming IER for interrupt on bit0 RCV holding Register\n");
  outportb(port+IER, 0x01);
  return TRUE;
* This is the test mode.
* It gets the address of the ports checks to see if they are there.
* Note: If a driver already exists I am not sure how to temporarily remove it.
* Well we will worry about it later.
* Warn the use to remove any drivers that are on the ports.
* Especially the mouse driver.
* pass the address to the test552 routine.
int test_mode()
      int i,i,k; /* generic variables */
      char port1[10], port2[10];
      int pt1,pt2; /* this are the integer port numbers */eviscost-as analosis for Bis time and getting about 11 to
      void test552();
      printf("WARNING: This program will not work if the ports to be tested\n");
```

printf("

APPLICATION NOTES

```
printf("
                  Please remove the drivers before doing this test.\n");
      while(TRUE) {
        printf("First Port Address (In HEX) > "):
        scanf("%s",port1);
        pt1 = strtol(port1.NULL.16):
        fflush(stdin):
         * Check if this port exists. else loop
         if(check_port(pt1))
         printf("Error: Port %4xH does not exist. Try again\n",pt1);
      while(TRUE) {
        printf("Second Port Address (In HEX) > ");
        scanf("%s",port2):
        pt2 = strtol(port2, NULL, 16);
        fflush(stdin);
        * Check if this port exists. else loop
        \*/
        if(check port(pt2))
         printf("Error: Port %4xH does not exist. Try again\n",pt2);
      /* Test 554 with the two port addresses */
      test552(pt1,pt2);
      return TRUE:
* It first generates a random number for the data size to be generated.
* Then generates a random data whose length is equal to the data size.
* It puts it out on both the ports and polls for the interrupt to occur.
* It reads both the ports until all characters are received OR a timeout repeated and any entire the last
* has occured. It then prints out the error Messages if any.
* This loop is done for ever.
\*/
```

have drivers installed in them. e.g Mouse driver\n");

```
void test552(p1,p2)
unsigned int p1, p2;
 int i,j,c,w,n;
 unsigned char outbuf[20], inbuf1[20], inbuf2[20];
 unsigned char pbuf[200];
 unsigned long timeout, pass;
 printf("ST16C552 External Loop Test Beginning\n");
 printf("Testing ports %4x and %4x\n\n", p1, p2);
 printf("Programing ports for 56K,8 bit,no parity,1 stop bit,FIFO trigger level 01\n");
 printf("This program uses POLLED mode for testing\n");
 printf("Press Cntrl-C to stop the testing and quit\n");
 printf("Note: The ports will remain at the above settings after the TEST\n");
 /* Programming ports for 8 bits, no parity, 56K baud, an 50 pavisour need and its films also eviscent
                            FIFO enabled at level 01 */
 /* Program first port */
 printf("Programming port %x4\n",p1);
 init_uart(p1, COM 56K, COM NOPARITY,
         _COM_CHR8_, COM_STOP1_,TRUE, COM_FIFO1_);
 /* Program Second Port */
 printf("Programming port %x4\n",p2);
 init_uart(p2,_COM_56K_,_COM_NOPARITY_, shoon = feet
         COM_CHR8 , COM STOP1 ,TRUE, COM FIFO1 );
 printf("Starting test\n");
 for (pass = 1;; pass++) {
      /* generate random size for data */
      n = rand():
      n += n >> 8:
      n \&= 0x0f;
      /* Make sure we never get a 0 as the random size data */
      if(n != 0x0f)
       n++;
      /* generate random data */
      for (w = 0; w < n; w++) {
           c = rand():
           c += c >> 8:
           c &= 0xff;
           c := 0x01 ; /* no NULLs allowed */
           outbuf[w] = c;
```

```
outbuf[w] = NULL;
printf("******* Pass %10ld Sending %d ******* \015", pass, n) :
/* Transmitt the data */
for (i = 0; i < n; i++) {
     outportb(p1, outbuffil):
     outportb(p2, outbuf[i]);
/* loop waiting for intr pending */
for (i = 0::i++) {
     if ((~inportb(p1+ISR) & 0x01) && (~inportb(p2+ISR) & 0x01))
          break:
/* receive data until all has been received OR timeout */
timeout = 0x0008F;
for (i = j = 0; ((i < 20) && (j < 20));) {
     if (inportb(p1+LSR) \& 0x01) inbuf1[i++] = inportb(p1);
     c = rand();
     c += c >> 8;
     c &= 0x001f;
     C++ ;
     for (; c != 0; c—);
     if (inportb(p2+LSR) \& 0x01) inbuf2[j++] = inportb(p2);
     if (timeout— == 0) break;
/* If timed out then print message else comparse data */
if(timeout == 0)
     printf("Timed out on Ports\n");
else {
  inbuf1[i] = inbuf2[j] = NULL;
  /* compare results */
  if (strcmp(outbuf, inbuf1) ;; ( i != n)) { Shall sale mechanied as 0 a lagrayed aware are also 1.5
       printf("\nError:%04x Sent: ", p2);
       for (w = 0; w < n; w++)
            printf(" %02x", outbuf[w]);
       printf("\n%04x Received:", p1);
       for (w = 0; w < i; w++)
           printf(" %02x", inbuf1[w]);
       printf("\n");
 if (strcmp(outbuf, inbuf2);; ( j != n )) {
       printf("\nError:%04x Sent: ", p1);
       for (w = 0; w < n; w++)
            printf(" %02x", outbuf[w]);
```

7

GENERAL APPLICATION NOTE FOR STARTECH CLOCK FAMILY

The ST49CXXX video / memory clock chips provide 5-130 MHz clock outputs which may cause unwanted EMI problems.

To minimize problems with meeting FCC EMI requirements, consideration should be given to the following sections of the board design.

Power supply conditioning
Printed Circuit Board Layout
Video / Memory clock outputs and drive capabilities
External clock sources
Reference clock sources
Digital control / select inputs
External loop filters

Power supply considerations

Under normal conditions no external components are required for propper operation of any of the internal circuitry of the ST49CXXX. It is required to have spike free (or minimum) and stable supply source to the chips. To provide stable and clean supply voltage to STARTECH clock chips we recommend to use $0.1 \mu F$ capacitors close to IC's power supply lines (VCC, AVCC and DVCC inputs). Analog and digital supply lines are separated from each other to reduce noise generated due to internal digital switching.

In most of the design cases +5V and +12V supplies are provided. A clean +5V supply can be obtained from the +12V supply by utilizing a 470Ω drop resistor and 5.1V zener diode bypassed by $0.047\mu F$ and $2.2\mu F$ Tantalum capacitors (or higher) to ground.

Trace width should be maximized from the supply source and good ground planes on top and bottom layers of the printed circuit board are recommended.

Printed Circuit Board (PCB) layout

We recommend to place all external components as close as possible to the clock chips to reduce trace length between pin and component connections. It is important to keep components not related to clock IC's (DRAM and other memory devices) far and not share the grounds. In applications utilizing a multi-layer board, GND, AGND, and DGND should be directly connected to the ground plane. If possible A full power and ground plane layout should be employed both under and around the IC package.

Video / Memory clock outputs and drive capabilities

Video clock is usually the highest frequency present in video graphics system board/card and consideration should be given to FCC EMI requirements.

The trace connecting DCLK and MCLK clock output pins to other components should be kept as close as possible (with optional 33Ω resistor in series) to reduce the possible emitting signals and jitter.

External clock sources

When an external clock source is used to bypass the internal VCO to DCLK and MCLK outputs, clock should have fast rise / fall times and minimum jitter. This signal will be connected internally to the clock output pin when it is selected / enabled. The internal VCO circuit will be locked to its internal selected frequency.

Reference clock sources

The internal oscillator circuit contains all of the passive components required for the external crystal. An appropriate parallel resonant crystal should be connected between XTAL1 and XTAL2.

The crystal leads and input pins should be maintained as close as possible, and the body of the crystal should be grounded to minimize the noise pickup. For IBM compatible applications, the 14.31818 MHz system or crystal clock is used as a reference clock to the chip.

Digital control / select inputs

The ST49CXXX provides TTL compatible address select and latch input pins to interface with CMOS or TTL/LSTTL devices. The A0-A4 and M0-M1 can also be connected to the Data bus if required.

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Power supply considerations

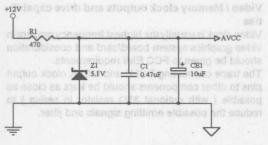
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1.0 Quality and Reliability information

The STARTECH semiconductor quality program starts with the design of new products. Each design circuit performance is verified using simulations over voltage and temperature values beyond those of specified product operation.

The design process includes consideration of quality issues such as signal levels, power dissipation, noise generated from internal clock circuits and testability of all device functions.

The STARTECH semiconductor document control department maintains control over all manufacturing specifications, lot travelers, procurement specifications and drawings and test programs.

HP Laserjet III

All changes of design are subject to approval by the Engineering, Quality and Manufacturing managers.

STARTECH semiconductor performs a thorough internal product qualification prior to the delivery of any new product or enhanced existing products other than prototypes/samples.

tion process to ORBIT semi sloot ngised ed 1.1 Sunnvysle. California Packaging and final esting are

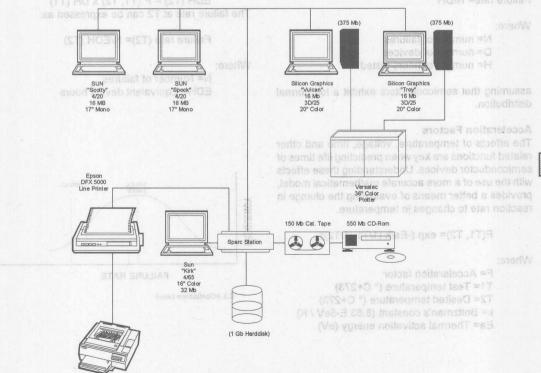
Schematics entry: Logic & Fault simulators:

Layout Synthesis:

Layout Editor: 8 betolbeig ed is Layout Verification:

View Logic Startech Advanced Logic simulator Goliath (Startech Layout synthesis)

Opal Dracula



8

150 samples from three different product lots are selected to perform extended temperature operation test, 85° C/ 85% R.H. / 5.5V temperature humidity bias. Same samples are used for accelerated burn-in and electro-static tests.

STARTECH semiconductor subcontracts its fabrication process to ORBIT semiconductor located in Sunnyvale, California. Packaging and final testing are also subcontracted to other vendors located locally or overseas.

1.2 Determination of the Failure Rate

In the simplest form, the failure rate prediction at a given temperature can be predicted as follows.

Failure rate= N/DH

Where:

N= number of failures
D= number of devices
H= number of hours tested

assuming that semiconductors exhibit a log normal distribution.

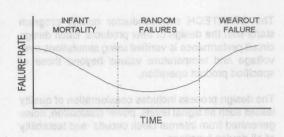
Acceleration Factors

The effects of temperature, voltage, time and other related functions are key when predicting life times of semiconductor devices. Understanding these effects with the use of a more accurate mathematical model, provides a better means of evaluating the change in reaction rate to changes in temperature.

F(T1, T2)= exp (-Ea/k (1/T1- 1/T2))

Where:

F= Acceleration factor
T1= Test temperature (° C+273)
T2= Desired temperature (° C+273)
k= Boltzman's constant (8.63 E-5eV / K)
Ea= Thermal activation energy (eV)



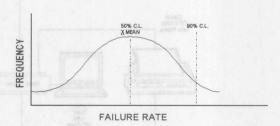
The equivalent device hours can be determined at temperature T2 can be expressed as:

EDH (T2) = F (T1, T2) \times DH (T1) The failure rate at T2 can be expressed as:

Failure rate (T2)= N/EDH (T2)

Where:

N= Number of failures EDH= Equivalent device hours



C.L.=Confidence Level

1.3 Activation Energies for Primary Failure Mechanisms

Failure Mechanism	Ea	
Contamination	1-1.4 eV	
Silicon Defects	0.5 eV	
Polarization	1 eV	
Oxide Breakdown	0.3 eV	
Aluminum Migration	0.5 eV	
Trapping	1 eV	

1.4 Definition and common test methods

Accelerated operating life stress

Accelerated operating life stressing is performed to accelerate failure mechanisms, which are thermally activated, through the application of extreme temperature and dynamic biasing conditions. The typical temperature and voltage conditions used in the stress are 125 °C with a bias level at the maximum data sheet specifications.

85 °C/ 85 % R.H.

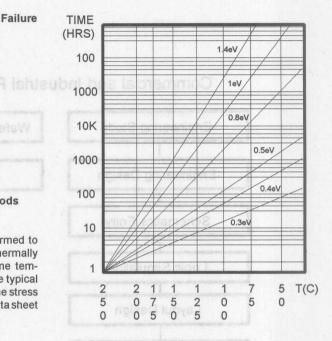
85 °C/ 85 % R.H. is an environmental stress performed at a temperature of 85 °C and relative humidity of 85%. The test is designed to measure the moisture resistance of encapsulated devices.

Electrostatic discharge testing

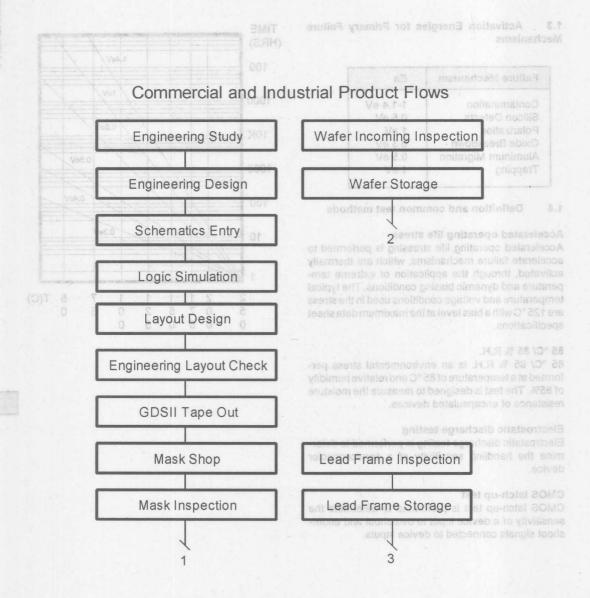
Electrostatic discharge testing is performed to determine the handling sensitivity of a semiconductor device.

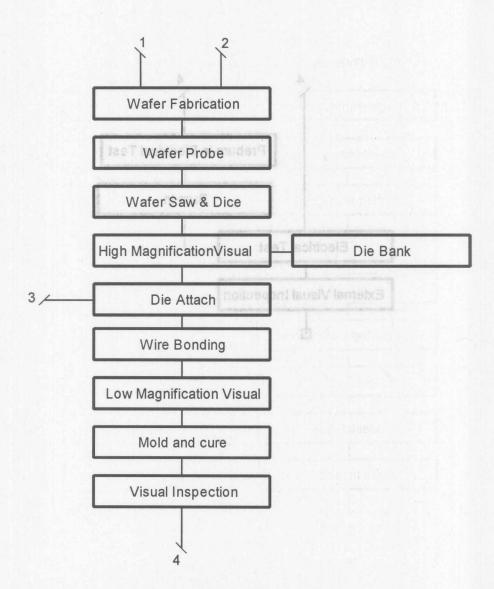
CMOS latch-up test

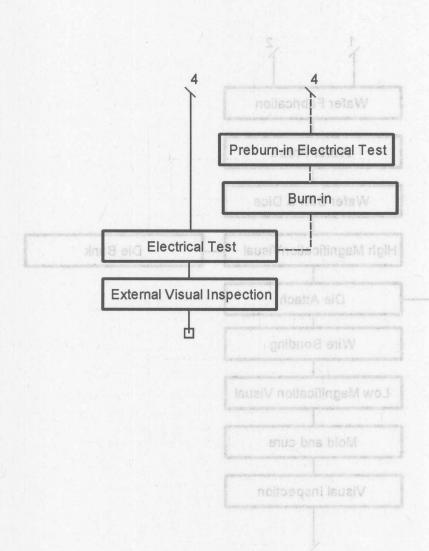
CMOS latch-up test is performed to determine the sensitivity of a device input to overshoot and undershoot signals connected to device inputs.

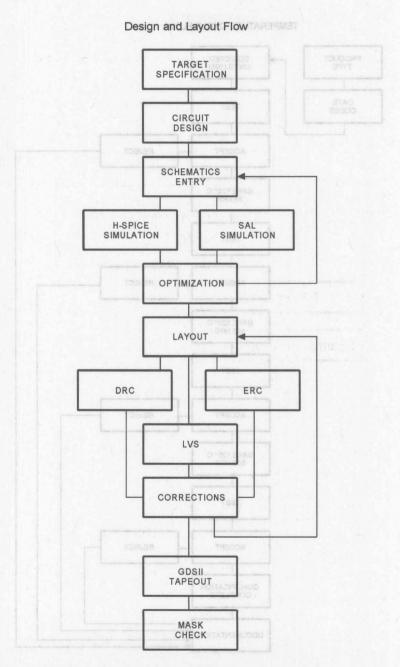




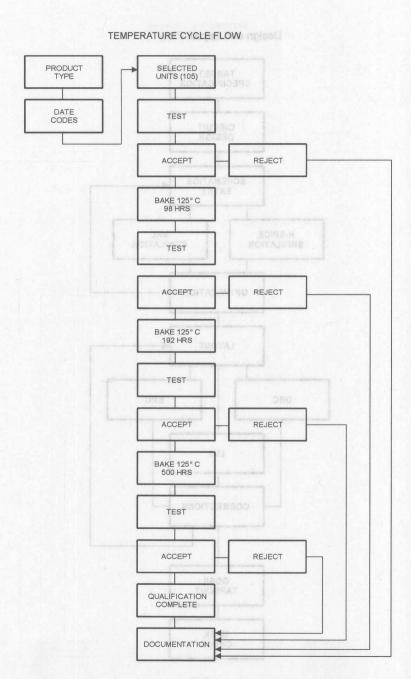










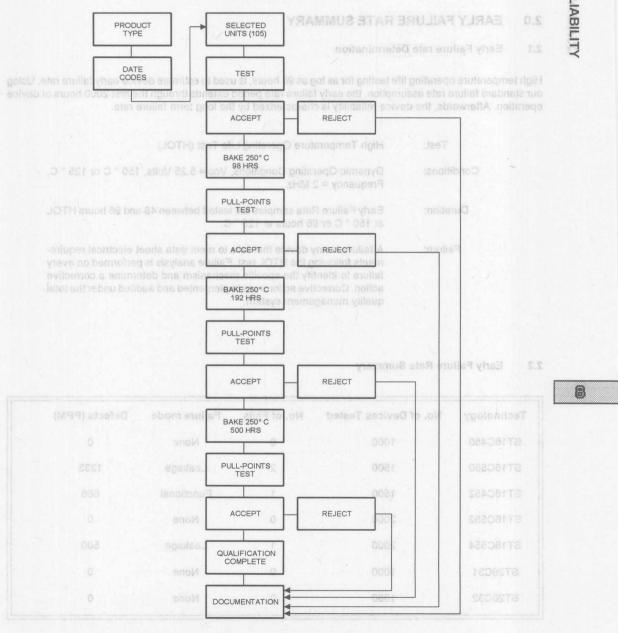


8-10

QUALITY / RELIABILITY

HIGH TEMPERATURE OPERATING LIFE

85 / 85 BIAS CYCLE FLOW



HIGH TEMPERATURE OPERATING LIFE

2.0 EARLY FAILURE RATE SUMMARY

2.1 Early Failure rate Determination

High temperature operating life testing for as log as 96 hours, is used to estimate device early failure rate. Using our standard failure rate assumption, the early failure rate period extends through the first 2000 hours of device operation. Afterwards, the device reliability is characterized by the long term failure rate.

Test:

High Temperature Operating Life Test (HTOL)

Conditions:

Dynamic Operating Conditions, Vcc = 5.25 Volts, 150 ° C or 125 ° C,

Frequency = 2 MHz.

Duration:

Early Failure Rate samples are tested between 48 and 96 hours HTOL

at 150 ° C or 96 hours at 125 ° C.

Failure:

A failure is any device that fails to meet data sheet electrical requirements following the HTOL test. Failure analysis is performed on every failure to identify the specific mechanism and determine a corrective action. Corrective actions are implemented and audited under the total

quality management system.

2.2 Early Failure Rate Summary

Technology	No. of Devices Tested	No. of Fails	Failure mode	Defects (PPM)
ST16C450	1000	0	None	0
ST16C550	1500	2017/04-133	Leakage	1333
ST16C452	1500	1	Functional	666
ST16C552	2000	0 193004	None	0
ST16C554	2000	1 MOTAGIPLAL		500
ST26C31	1000	0	None	. 0
ST26C32	1000	0	None	0

3.0 LONG TERM FAILURE RATE SUMMARY YOASTS SAUTARSMST HOW

3.1 con Long Term Failure Rate Determination as of beau at least shill shall ybes to shufe agree T daily shill

A High temperature Operating Life test is used to estimate long term reliability. By operating the devices at accelerated temperature and voltage, hundreds of thousands of use hours can be compressed into thousands of test hours. The method used to estimate failure rates from stress data is summarized.

Test: High Temperature Operating Life Test (HTOL)

Conditions: Dynamic Operating Conditions, Vcc = 5.25 Volts, 150 ° C, Frequency

= 2 MHz.

Duration: Long term Failure Rate is minimum 168 hours HTOL at 150 ° C

periodically tested to 2000 hours.

Reliability: Failure mechanisms common to semiconductor components are accel-

erated by temperature and voltage. In calculating failure rates, though,

only temperature acceleration is included.

3.2 Long term Failure Rate Summary

Technology	No. of Devices Tested	No. of Fails	Failure mode	Defects (PPM)
ST16C450	5000	1	Functional	200
ST16C550	8000	1	Leakage	125
ST16C452	7500	Ker Tes ⁰ (PCT)	None	0 Test
ST16C552	5000	° C, M ⁰ bies, 298	None	Co-Omions:
ST16C554	7000	Cooker feet is a r	Functional	143
ST26C31	1000	re environmente acks, lo coontar	None	0
ST26C32	1000	d by this stress.	None	0



4.0 HIGH TEMPERATURE STEADY STATE LIFE TEST 38U JAF M99T 040J

The High Temperature Steady State Life test is used to accelerated ionic contamination problems. Static bias is used because a constant voltage gradient accelerated diffusion of ionic species. The method used to estimate failure rates from stress data is summarized.

Technology	No. of Devices Tested	No. of Fails	Failure mode	Defects (PPM)
ST16C450	3000 H) J25T 51	ature Operating Li	Functional	333 Test
ST16C550	Vcc = 5.2000Els, 150 °C,	erating (Onditions	None	Co 0 ditions:
ST16C452	4500	1	Functional	222
ST16C552	1000 and 381 mumin	asted to 0.000 hour		0
	semicond 0001 components			R o ability:
ST26C31	ige. In celculating failure rate s included 0001	perature and voltature acromation i		0
ST26C32	1000	0	None	0

5.0 PACKAGE STRESS TESTS

Test:

Startech Semiconductor Reliability qualifies and continuously monitors the packaging reliability to ensure exceptional resistance to environmental stress. Package reliability stress testing and failure rates are summarized.

Pressure Cooker Test (PCT)

5.1 Pressure Cooker Test

Conditions: 15 PSIG, 120 ° C, No bias, 295 hours minimum time

The Pressure Cooker Test is a highly accelerated packaging stress test used to ensure environmental durability of epoxy packaged parts. Passivation cracks, ionic contamination and corrosion susceptibility are all accelerated by this stress.

Failure: Any device which fails to meet all data sheet requirements is classified as a failure.

5.2 Pressure Cooker Summary

Technology	No. of Devices Tested	No. of Fails	Failure mode	Defects (PPM)
ST16C450CP40	5000	01	Functional	200
ST16C450CJ44	5000	0	None	ST16C450CJ 0
ST16C550CP40	5000	0	None	TIECSSOCP 0
ST16C550CJ44	5000	1	Leakage	200
ST16C452CP68	5000	01	Functional	200
ST16C552CP68	5000	01	Functional	200 OSSOCIT
ST16C554CP68	5000	0	None	T16CS54CP6
ST26C31CP16	1000	0	None	37280310916
ST26C32CP16	1000	0	None	ST28C32CP10

5.2 Highly Accelerated Stress Test

Test: High Accelerated Stress Test (HAST)

Conditions: 18.6 PSIG, 125 °C, 85% RH, 5.5 Volts bias, minimum test time, 96

hours.

Purpose: HAST is an accelerated biased humidity test that literature, and tests

run at Startech, has shown provides an acceleration 10-15X over 85 ° C/85%. This test provides the factory with rapid feedback regarding the

quality of the epoxy package process.

Failure: A failure is defined as a device which fails to pass the standard data

sheet test program.

5.4 Accelerated Stress Summary

Technology	No. of Devices Tested	No. of Fails	Failure mode	Defects (PPM)
ST16C450CP40	5000	0	None	0.7002430FT
ST16C450CJ44	5000	0	None	STIECASOCI O
ST16C550CP40	5000	0	None	O-GOOGEOGET
ST16C550CJ44	5000	0	None	TIBOSSOCI O
ST16C452CP68	5000	0	None	T16C452CP.0
ST16C552CP68	5000	0	None	TIBOSSZOF 0
ST16C554CP68	5000	0	None	TIBOSSIOPIO
ST26C31CP16	1000	0	None	stzecsicei0
ST26C32CP16	1000	0	None	0 93983857

5.5 Temperature Cycle Test

Differences in thermal expansion coefficients are accentuated by cycling devices through temperature extremes. If the materials do not expand and contact equally, large stresses can develop.

Temperature Cycle
MIL-STD-883C, Method test stress mechanical integrity by exposing a device to alternating temperature extremes. Weakness and thermal expansion mismatches in die interconnections, die attach, and wire bonds are often detected with this acceleration test.
100 cycles minimum, periodically tested to 1000 cycles
Any device which fails to meet all data sheet requirements is classified as a failure.

ESD AND LATCH-UP

5.6 Temperature Cycle Summary

			dvs.	sente division
Technology	No. of Devices Tested	No. of Fails	Failure mode	Defects (PPM)
ST16C450CP40	5000	0 viivii	None None	0
ST16C450CJ44	5000	0	None	0
	= enuising 5000	cc = 3.07.0 Volt		0
ST16C550CJ44	5000	2	Leakage	400
	s. Latch-up has historicall			
ST16C452CP68	5000	lated wi 0 CMOS	None	0
ST16C552CP68	5000	ch fails 0 e Laten	None	0
		ine		
ST16C554CP68	5000	0	None	0
ST26C31CP16	1000	0	None	0
ST26C32CP16	1000	0	None	0 :210269

2

ESD AND LATCH-UP TEST

6.0 Latch-up Sensitive

Test:

Latch-up Sensitivity

Conditions:

Current Injection = 200mA Trigger, Hot Socket = Vcc 0-7 Volts, Vcc

Oscillation at Vcc = 3.5-7.0 Volts at 1 MHz, Temperature = 150 ° C.

Purpose:

The latch-up test is designed to test resistance of the devices to extreme

voltage and current excursions. Latch-up has historically been a

problem associated with CMOS devices.

Failure:

Any device which fails the Latch-up test if Latch-up occurs at less than

200mA of current.

6.1 Results:

All products are tested for latch-up during qualification.

Outputs:

All outputs are tested using a hot socket technique where the full voltage is applied instantly, on a voltage ramp, where voltage is increased

slowly. During the hot socket technique, a maximum of 400 mA was

allowed in order to protect the outputs from overstress.

Inputs:

All inputs are tested using both the hot socket technique and the voltage

ramp technique.

6.2 Conclusion:

Startech Semiconductor products are very resistant to latch-up.

7.0 Electrostatic Discharge (ESD)

Test: Electrostatic Discharge

Conditions: MIL-STD-883C, Method 3015

Purpose: The ESD test established the sensitive of device to electrostatic

discharge of the type than can occur during ordinary handling.

Failure: A device fails the ESD stress test is any pin combination defined in

method 3015 of MIL-STD-883C is damaged after testing with a 2000 Volts discharge. Data sheet electrical testing is performed to determine

if a device has been damaged.

7.1 Results:

All Startech Semiconductor products are tested for resistance to ESD during qualification. All pins pass ESD testing at 2000 Volts.

7.2 Conclusion:

Startech Semiconductor products are not ESD sensitive per the definition of MIL-STD-883C.



7.0 Electrostatic Discharge (ESD)

Test: Electrostatic Discharg

Conditions: MIL-STD-883C, Melhod 3011

Surpose: The ESD test established the sensitive of device to electrostatic

discharge of the type than can occur during ordinary handling.

A device fails the ESD stress test is any oin combination defined in method 3015 of Mit-STD-883C is damaged effecting with a 2000 Volts discharge. Data sheat electrical testing is performed to determine it is device has been demaged.

7.1 Regults:

All Starteon Semiconductor products are tested for resistance to ESD during qualification. All pins pass ESD testing at 2000 Volts.

7.2 Conclusion:

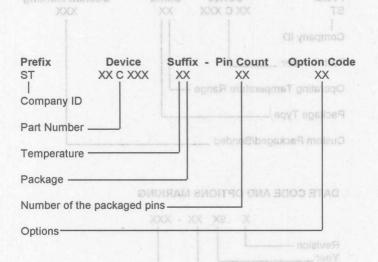
Startach Semicrophysias products are not ESD sensitive per the definition of Mill-STD-888C.

ORDERING INFORMATION 9

-ORDERING INFORMATION

PACKAGE MARKING INFORMATION (EXCEPT CLOCK SYNTHESIZERS AND TOFP PACKAGES)

ORDERING INFORMATION AND PART NUMBERING GUIDE .



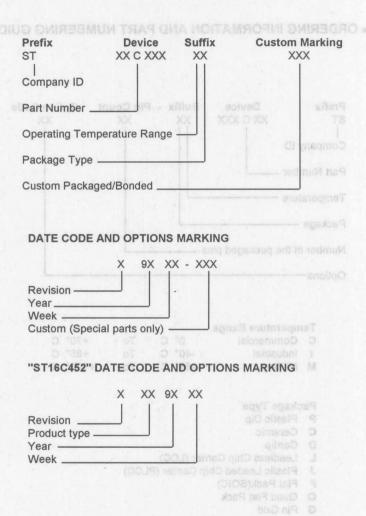
Temperature Range

C Commercial 0° C To +70° C
I Industrial -40° C To +85° C
M Military -55° C To +125° C

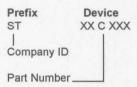
Package Type

- P Plastic Dip
- C Ceramic
- D Cerdip
- L Leadless Chip Carrier (LCC)
- J Plastic Leaded Chip Carrier (PLCC)
- F Flat Pack(SOIC)
- Q Quad Flat Pack
- G Pin Grid
- T Thin Shrink Small Outline Package (TSSOP)

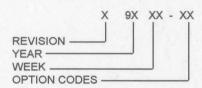
PACKAGE MARKING INFORMATION (EXCEPT CLOCK SYNTHESIZERS AND TQFP PACKAGES)



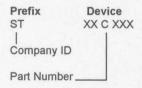
PACKAGE MARKING INFORMATION ... (CLOCK SYNTHESIZERS)



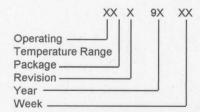
DATE CODE AND OPTIONS MARKING



48-TQFP PACKAGE MARKING INFORMATION =



DATE CODE AND OPTIONS MARKING



PACKAGE MARKING INFORMATION (CLOCK SYNTHESIZERS)

Prefix Device
ST XX C XXX
Company ID

DATE CODE AND OPTIONS MARKING

REVISION LAR WEEK WEEK OPTION CODES

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DATE CODE AND OPTIONS MARKING

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Revision —
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Week

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